Chapter- 3

< Semiconductor Diode > → (Duty cycle pros)

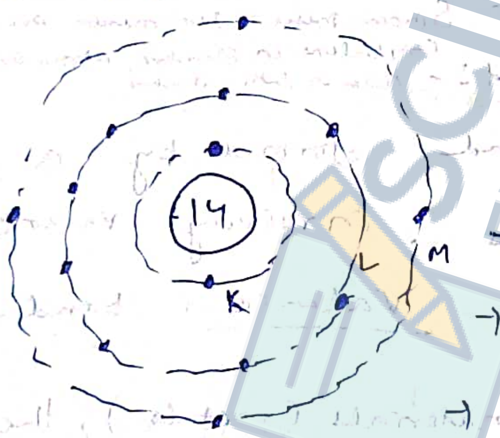
→ Bohr's atomic Model

→ Materials can be classified into 3 types depending upon the conductivity

(a) Conductor
(b) Semiconductor
(c) Insulator.

→ In electronics we will focus only on semiconductor.

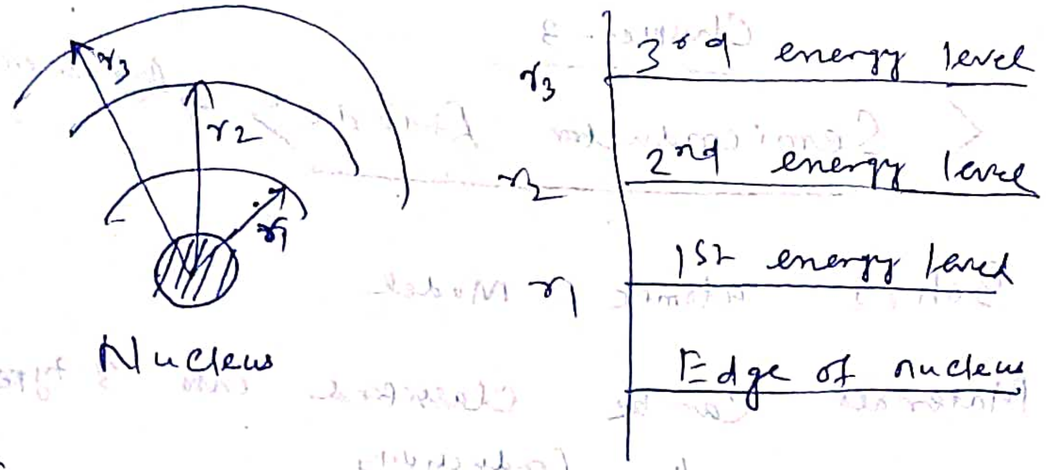
→ Consider a semiconductor material Silicon (Si). It has atomic no 14.



→ Electronic Configuration (2, 8, 4)

→ 2 electrons in K shell,
→ 8 " " L shell,
→ 4 " in M shell.

→ Each orbit has fixed amount of energy associated with it. The electrons moving in a particular orbit possess the energy of the orbit. Larger the orbit greater e's its energy. So outer orbit electrons possess more energy than inner orbit electrons.



Energy Bands :-

The electrons in the inner shells / orbits are strongly bounded to their nuclei while the electrons in the outermost shell / orbit, are not strongly bounded to the nuclei.

The electrons in the outermost shell of an atom are known as valance electrons.

Valance Band :- Since metal & semiconductor are Crystalline in Structure, atoms are closer in lattice structure.

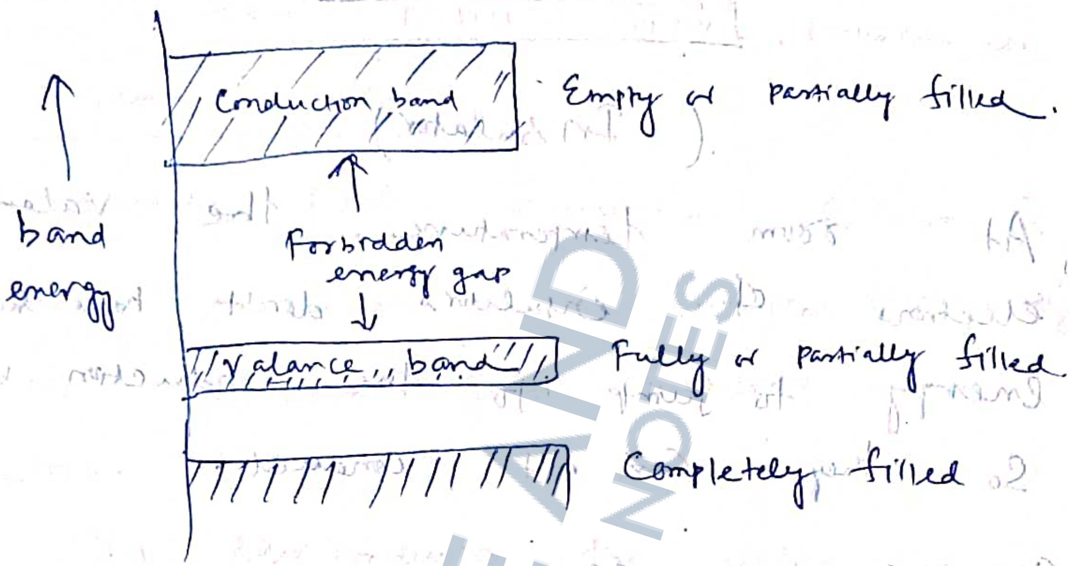
The ~~energy~~ band formed by a series of energy levels involving valance electrons (4 adjoining atoms) is known as Valance band.

Conduction Band :-

In certain materials (metals), the valance electrons are loosely attached to the nucleus. Even at ordinary temperature some of the valance electrons may leave the valance band and becomes free. These are called free electrons. These free electrons are responsible for conduction of current in a conductor & hence called as

Conduction electrons.

The band occupied by the conduction electrons is known as conduction band.



(Energy bands in solid.)

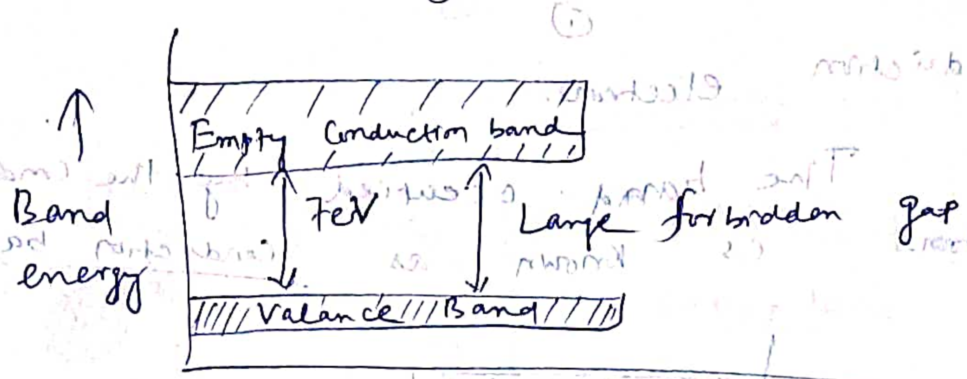
Forbidden Energy gap :-

The separation between conduction band and valance band is known as forbidden energy gap.

Classification of Solids:-

(i) Insulators:-

Insulators are those substances which prohibits the passage of electric current through them. In terms of energy band, the valance band is full while conduction band is empty. The energy gap between valence and conduction band is very large (e.g 7 eV).



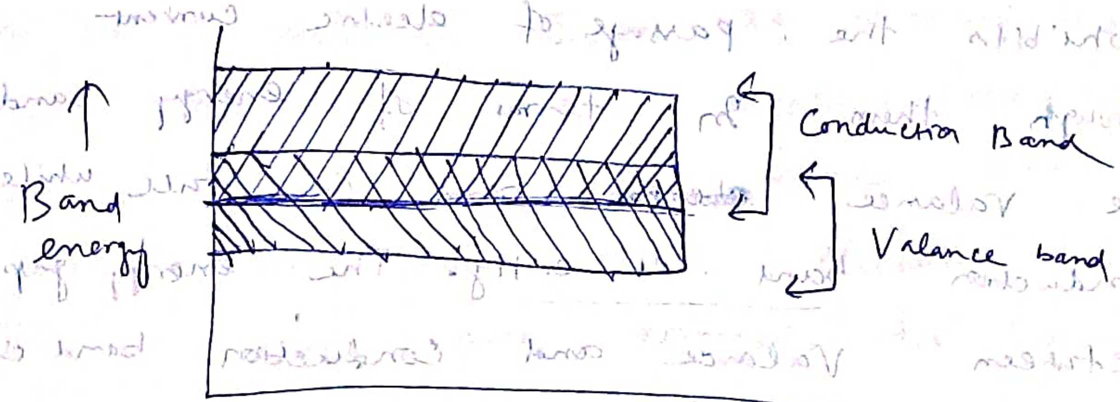
(Insulator)

At room temperature, the valance electrons of insulators don't have sufficient energy to jump to the conduction band. So they can n't conduct.

(ii) Conductor

Conductors are those substances which easey permit the passage of electric current through them.

This is because there is large number of free electrons available in a conductor. In terms of energy band, there is no forbidden gap. Valance band and conduction bands overlap with each other.



Because of this overlapping, a slight potential difference across a conductor causes free electrons to constitute electric current.

Ex :- Metals, Copper, Aluminium etc.

(iii) Semiconductors :-

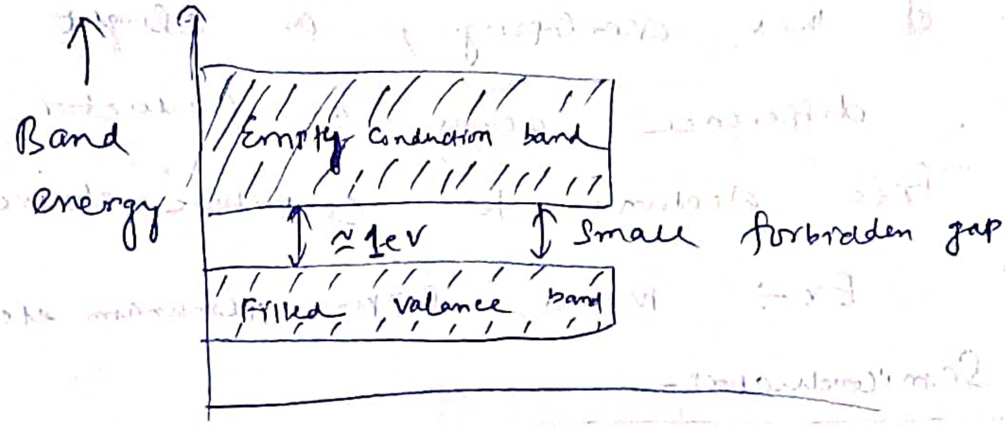
Semiconductor (e.g. Germanium, Silicon) are those substances whose electrical conductivity lies in between good conductors and insulators.

In semiconductor, the valance band is almost filled and conduction band is almost empty and the energy gap betⁿ valance and conduction band is very small.

BPUT Effect of temperature on semiconductor :-

At low temperature (0 K), the valance band is completely filled & conduction band is completely empty. So semiconductor behave as insulator at low temperature.

At room temperature, some electrons jump to conduction band and provide little conductivity. At temperature increases, more valance electrons jump to conduction band and conductivity of semiconductor increases. So electrical conductivity of a semiconductor increases with rise in temperature.



→ for 'Ge' energy gap → 0.72 eV
'Si' " " → 1.1 eV.

Bonds in semiconductor:-

→ In semiconductor, the covalent bond exist among the atoms.

→ Semiconductor material falls into 2 classes

→ Single crystal (Ge, Si)

→ Compound (GaAs, CdS, GaN, GaAsP)

↳ Compound of 2 or more semiconductor material.

GaAsP → Galium Arsenide Phosphide.

→ Frequently used → Ge, Si, GaAs

→ 'Si' is plentyly available in earth and it has high thermal stability. It can work in high temperature.

→ GaAs is 5 times faster than Si

Types of Semiconductor

- → Intrinsic Semiconductor
- → Extrinsic Semiconductor

Intrinsic Semiconductor:-

A semiconductor in an extremely pure form is known as intrinsic semiconductor.

Extrinsic Semiconductor:-

At room temperature, the intrinsic semiconductor has little current conduction capability.

To increase the conductivity of semiconductor, a small amount of impurity is added. The added impurity is of the order one atom per thousands of million of atoms of the pure semiconductor (for ex:- 1 ~~atom~~ impurity atom in 10^8 pure semiconductor atom)

The process of adding impurity atom to the intrinsic (pure) semiconductor is called doping. The semiconductor material that has been subjected to the doping process is called extrinsic semiconductor.

Intrinsic semiconductor (example / electronic configuration)

Si → (Silicon) ⇒ 14 → 2, 8, 4

Ge → (Germanium) → 32 → 2, 8, 18, 4

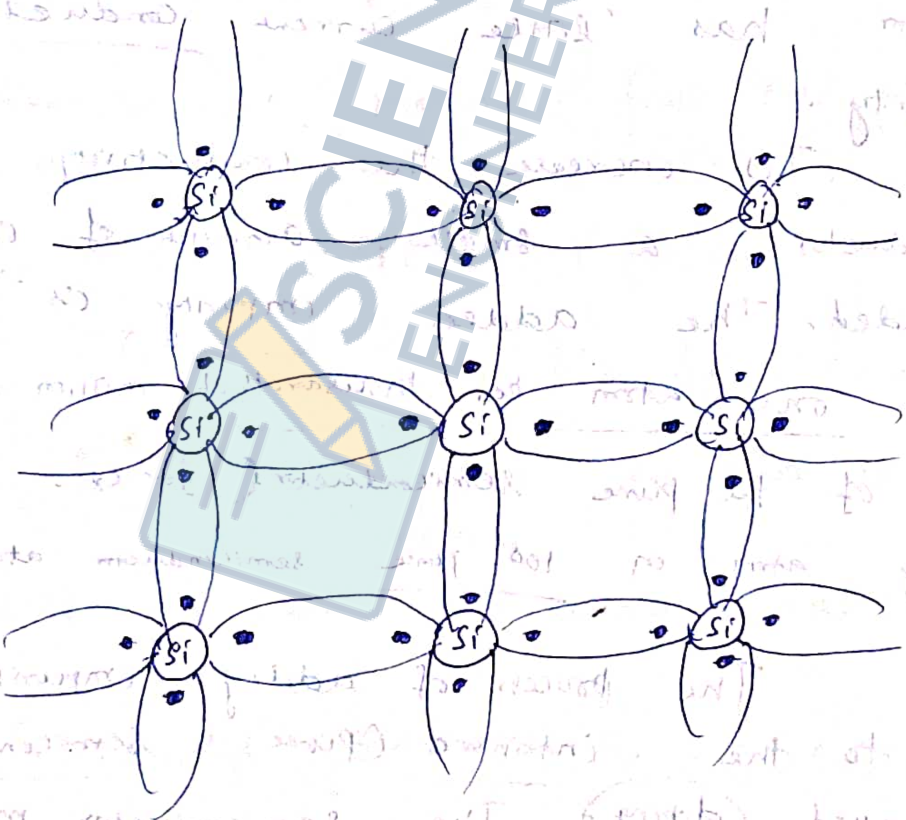
Ga → (Galium) → 31 → 2, 8, 18, 3

As → (Arsenic) → 33 → 2, 8, 18, 5

→ Atoms having 4 valance electrons called Tetra valent atoms.

→ 5 valance electrons → Penta valent atom

→ 3 valance electrons → trivalent atom.



< Covalant bonding of 'Si' atom >

Extrinsic Semiconductor types

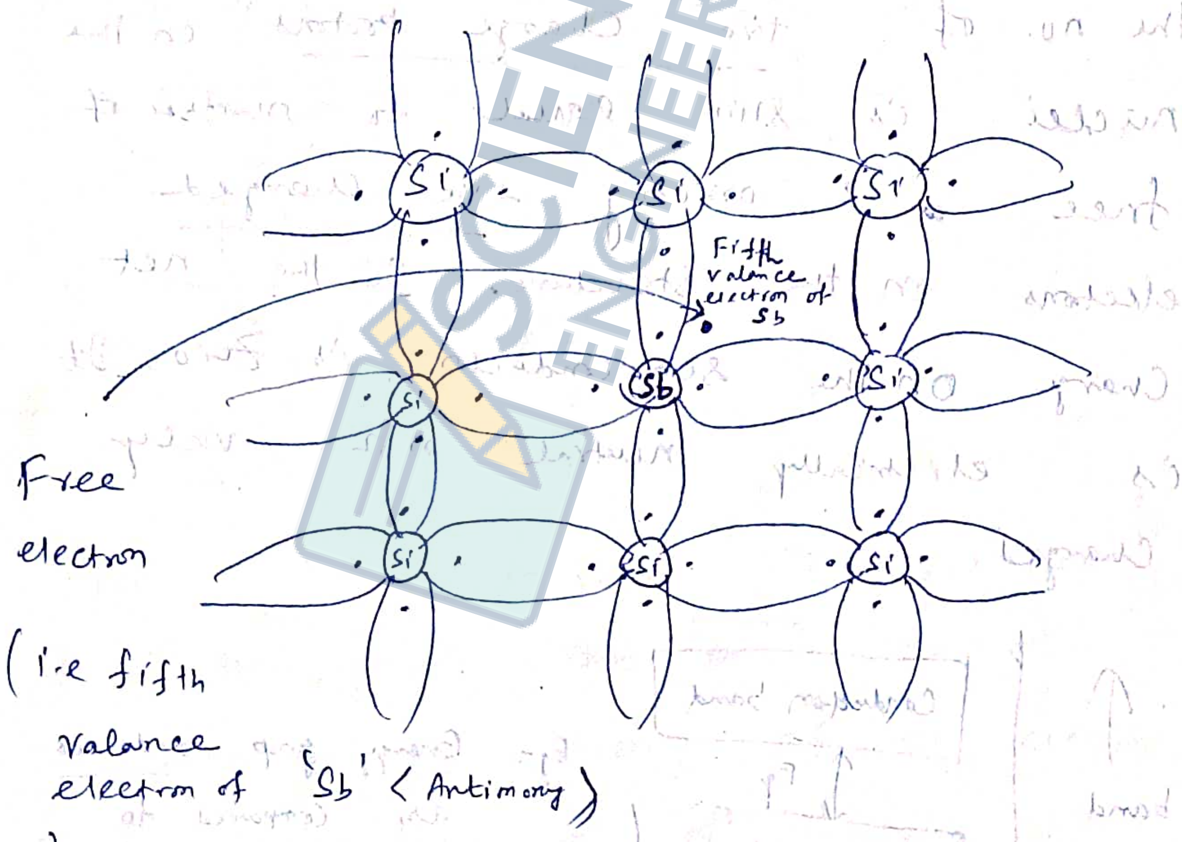
(i) N-type semiconductor.

(ii) P-type semiconductor.

N-type :-

If a small amount of pentavalent impurity is added to a pure semiconductor the resulting semiconductor is known as N-type semiconductor.

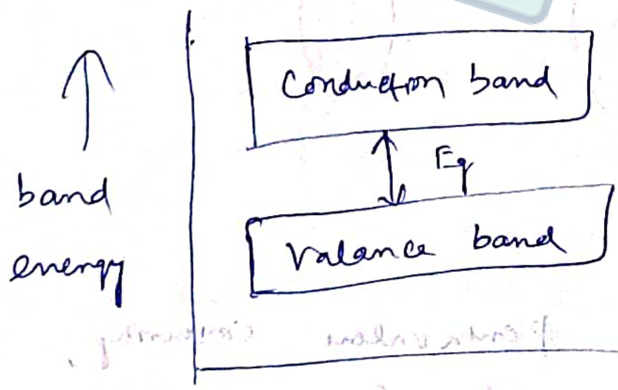
ex. of pentavalent impurity → (P, As, Sb)



→ The addition of pentavalent impurity, results in large no of free electrons because every impurity atom (penta valent) donate one electron. These electrons are loosely bounded to ~~these~~ its parent atom, and relatively free to move within the newly formed n type material.

N-type → N → stands for Negative (Since there are large no of free electrons produced in N type semiconductor)

→ Though large no. of free electrons present in n-type material, it is still electrically neutral. Ideally the no. of +ve charge protons in the nuclei is still equal to number of free & orbiting -ve charged electrons in the structure. So the net charge on the semiconductor is zero. It is electrically neutral not -vely charged.

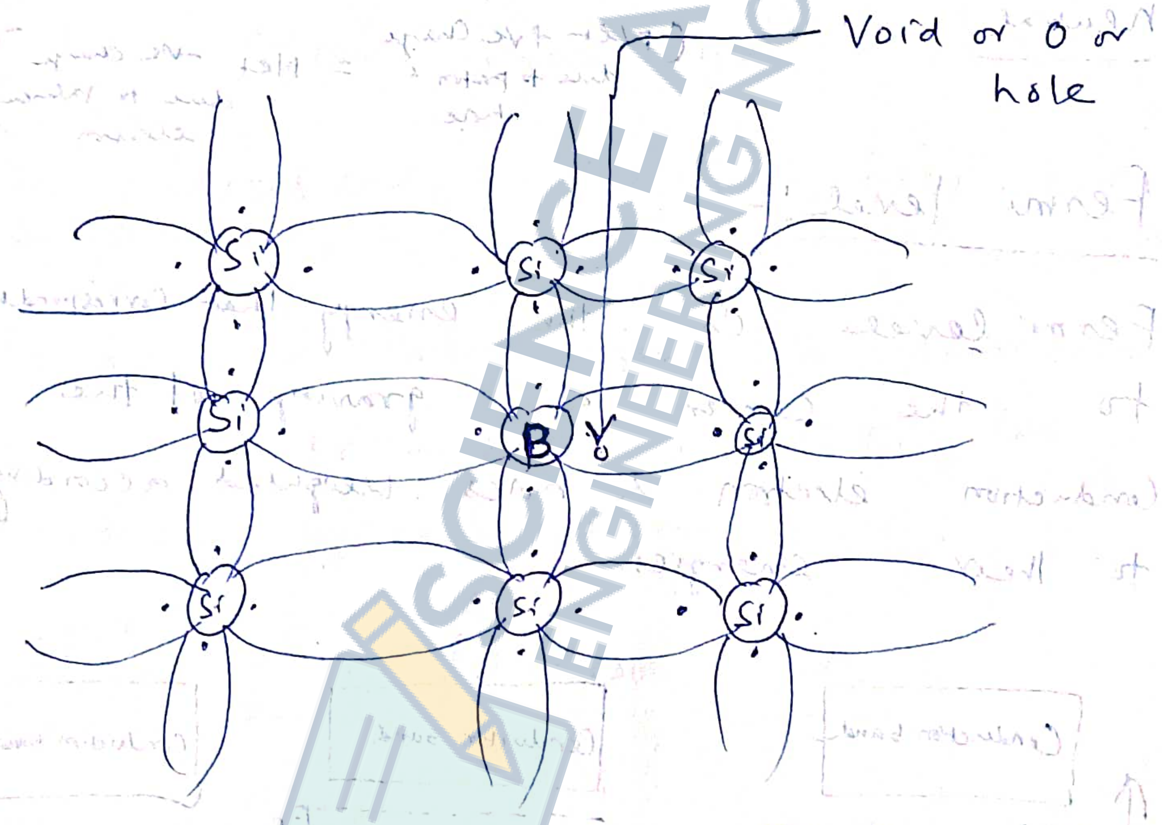


Eg = Energy gap reduces as compared to intrinsic semiconductor.

P Type semiconductor:-

When a small amount of trivalent impurity is added to a pure semiconductor during the crystal growth, the resulting crystal is called p-type semiconductor.

Trivalent impurity:- (Boron, Aluminium, Galium, Indium i.e B, Al, Ga, In)



Since the trivalent impurity has 3 covalent bonds, fourth bond of Si atom is missing of one electron. The vaccancy of this electron is called a hole.

P type → P stands for Positive.

Since holes are the absence of electron they are the +ve charge carriers.

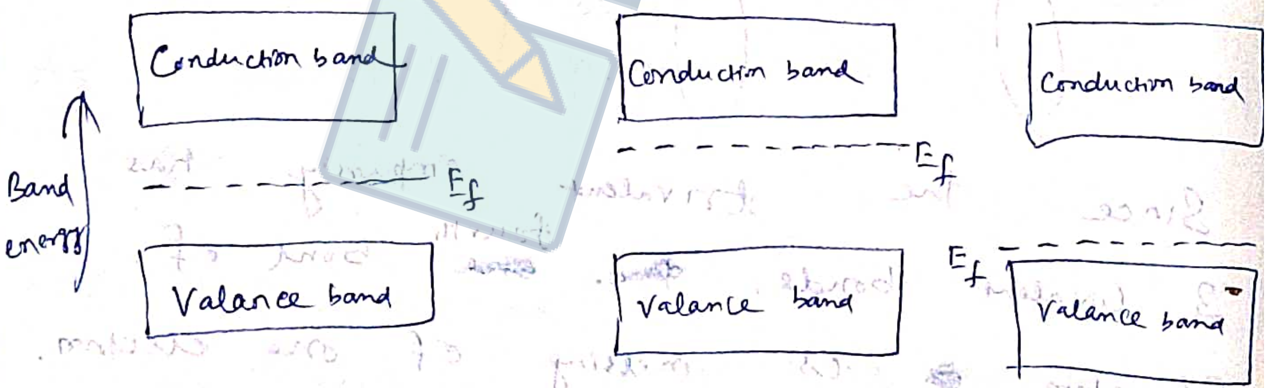
Since the semiconductor has plenty of holes (+ve charge carriers) it is called P-Type semiconductor.

→ Though it consists of large no. of holes, it is still electrically neutral.

(Net +ve charge due to proton & hole = Net -ve charge due to valance electron)

Fermi level :-

Fermi level is the energy that corresponds to the center of gravity of the conduction electron & holes weighted according to their energies.



(Intrinsic) (N-type) (P-type)

→ For intrinsic semiconductor Fermi level stands exactly in the middle of the forbidden energy gap.

→ For n type the Fermi level is towards the conduction band & for P-type it shifts towards to the valance band.

Fermi-Dirac function

$$f(E) = \frac{1}{1 + e^{\left(\frac{E - E_f}{KT}\right)}}$$

E_f = Fermi level energy.

At Fermi level, $E = E_f$, $f(E) = \frac{1}{1+e^0} = \frac{1}{2}$

Thus, an energy state at fermi level has a probability of $\frac{1}{2}$ of being occupied by an electron.

Donor ion & Acceptor ion

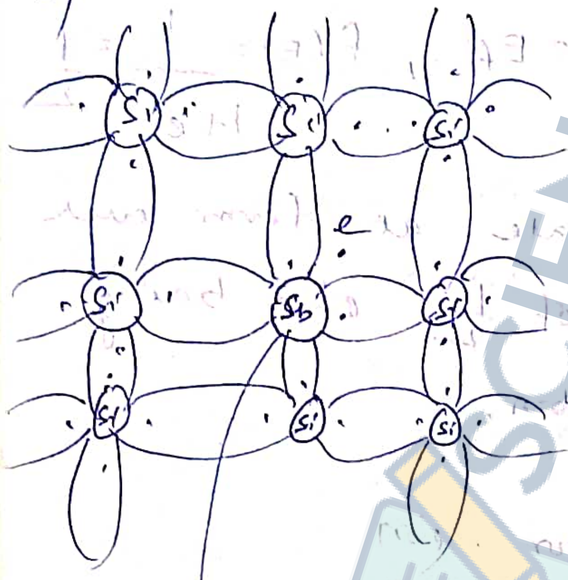
Donor ion	Acceptor ion
1) The pentavalent doping atoms are known as donor atoms.	1) The trivalent doping atoms are known as acceptor atom.
2) Because the pentavalent atom donate one electron.	2) Because the hole generated can accept the electron or the trivalent atom can accept one electron.

3) After donating an electron the atom becomes +ve.

4) So donor atoms are +vely charged.

5) They are denoted by ⊕

6)



Donor atom ⊕

Note:-

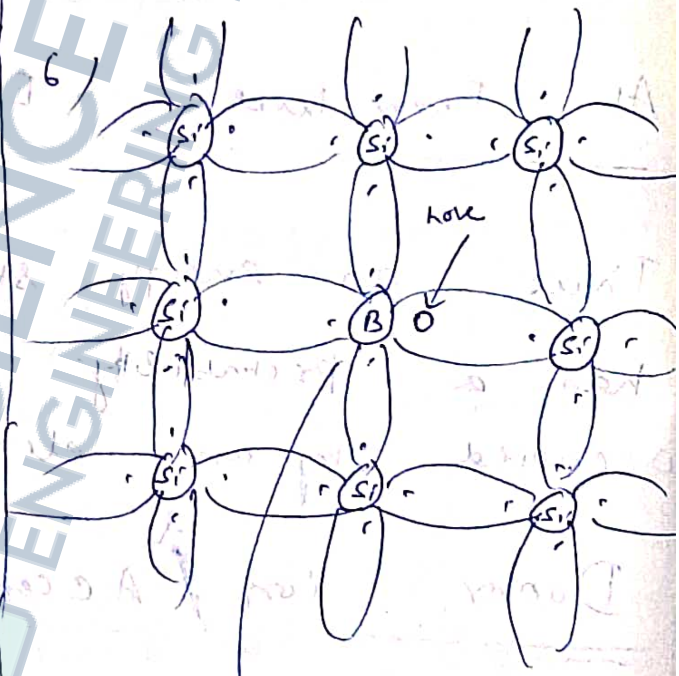
Trick:- DONOR ion → In N type semiconductor

3) After accepting one electron the atom becomes -ve.

4) Acceptor atoms are -vely charged.

5) They are denoted by ⊖

6)



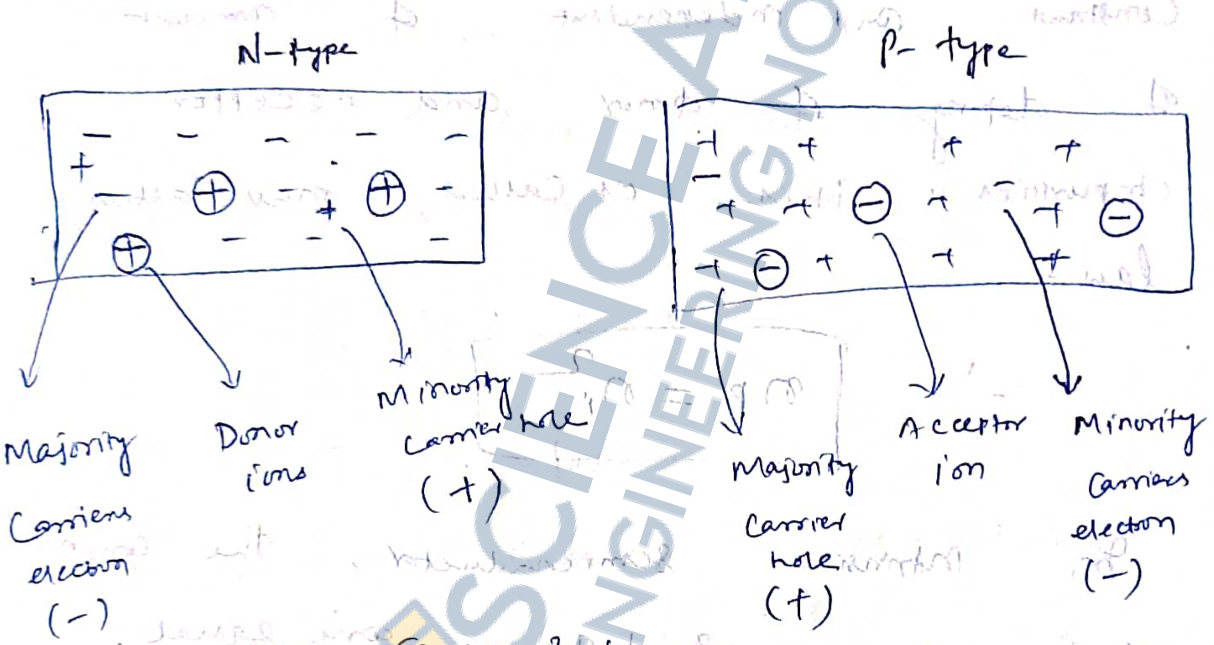
Acceptor atom ⊖

Trick:- Acceptor → In P type semiconductor.

Majority & Minority Carriers:-

→ In n type materials electrons are the majority carriers and holes are the minority carriers.

→ In p type materials holes are the majority carriers & electrons are the minority carriers.



Mobile Charge Carriers & Immobile ions

→ The ions in the n type semiconductor i.e donor ions are fixed in the crystal. So they are immobile ions and can't take part in conduction.

→ Similarly in P type semiconductor the acceptor ions are immobile, they are fixed in the crystal & can't take part in conduction.

Mass Action law

Let n_i = Intrinsic concentration

n = Concentration of electron

p = Concentration of hole.

- At thermal equilibrium, the product of Concⁿ of hole & electron is a constant and independent of amount of doping of donor and acceptor impurities. This is called mass action law.

∴
$$\boxed{np = n_i^2}$$

In intrinsic semiconductor, the concⁿ of electron & hole are equal. $(n = p = n_i)$

In n type, electron concⁿ increases & hole concⁿ decreases but their product remain const.

In p type, hole concⁿ increase, & electron concⁿ decreases but their product remain constant.

~~Diffusion~~ :-

Drift :-

When a electric field is applied across a piece of semiconductor, the electron & holes get accelerated ~~...~~

The velocity acquired by them is called drift velocity.

If Electric field (E) is applied across the semiconductor,

$$v_{drift} \propto E$$

$$\Rightarrow v_d = \mu E$$

μ is a constant called mobility.

So mobility is defined as the drift velocity per unit electric field.

$$\mu = \frac{v_d}{E}$$

Unit of μ:

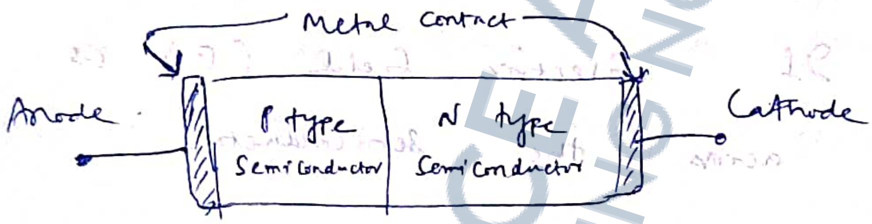
$$\mu = \frac{m/sec}{volt/meter} = \frac{meter}{sec} \times \frac{meter}{volt}$$

$$\text{Unit of mobility} = \frac{(meter)^2}{volt \cdot sec}$$

P-N Junction Diode:-

~~Wh~~ If in a single piece of semiconductor material (Ge or Si) one half is doped with p type impurity and other half ~~is~~ is doped with n type impurity, then P-N junction diode is formed.

The plane dividing the 2 halves or zone is called P-N junction.



Symbol:-

Diode → Di-ode
└→ 2 terminals (+ve and -ve)

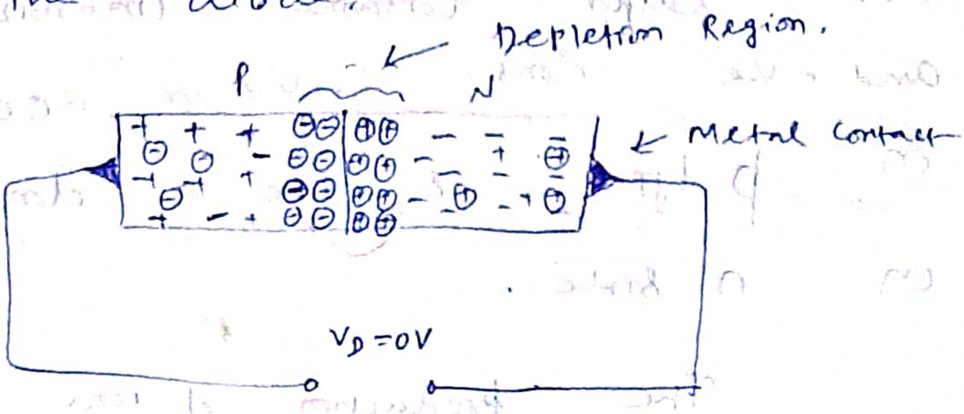
Symbol: →|—

The symbol is like a arrow mark. The arrow mark show the direction of current flow.

Physical Operation of P-N Junction Diode

Case-I :- When no voltage is applied

across the diode.



Formation of depletion Layer:-

Suppose the P-N junction is just formed. At this instant, holes are in P-region & electrons are in N region. However, there is greater concentration of holes in P-region than N-region. Similar case for electron, greater concⁿ in N-region than P-region.

Due to the difference in concentration holes flows from P to N and electrons flows from N to P. This process is called diffusion.

In the diffusion process, holes & electrons terminate their existance by recombination. Due to recombination a narrow region is formed at the junction called depletion layer. It is so called because this region is devoided or depleted of free and mobile change carriers because

This layer contains immobile +ve and -ve ions. -ve or acceptor ion in p type & +ve or donor ion on n side.

The production of ions at the junction is due to the fact that the impurity atoms which provide electron & holes, themselves left behind as +ve & -ve ions.

→ when electron leaves, it left behind a +ve ion & when hole leaves it left behind a -ve ion.

→ The ions are immobile or fixed on their position, ~~They~~ The +ve & -ve uncovered charges generate an electric field across the junction directed from n side to p side. This electric field developed across the junction don't allow for further flow of carriers.

In other way :-

The +ve charge on n side repels the holes to cross from p side to n side and -ve charge on p side repels the electron to enter from n type to p type. Thus a ~~barrier~~

a barrier is set up against further movement of charge carriers. This is called potential barrier or junction barrier V_0. This barrier potential is of the order 0.3 V for 'Ge' and 0.7 V for 'Si'.

Reverse Biasing:-

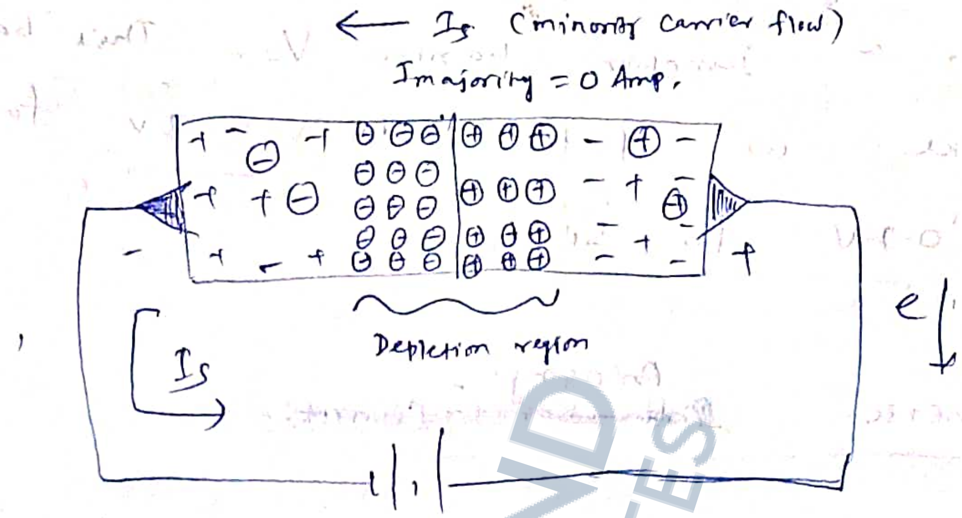
Bias:- The term bias refers to the application of an external voltage across the 2 terminals of the device to extract the response.

If no bias is applied the net current flow in one direction is zero.

Reverse bias:-

When an external potential of V volts is applied across the P-N junction such that +ve terminal of the battery is connected to the n type material & -ve terminal is connected to the p type material, then it is called reverse biasing.

In this case, the number of uncovered +ve ion in the depletion region of n type material will increase due to large no. of free electrons drawn to the +ve terminal of applied voltage. Same the case -ve ions increase in p type.



The net effect, therefore is a widening of depletion region. This widening of depletion region will establish too great barrier for majority carriers, effectively the majority carrier current flow is zero.

Reverse saturation current (I_s) :-

There are certain minority carriers present in p type & n type semiconductor.

· Thermally generated holes in the n type material diffuse through n material to the edge of depletion region. Therefore, they experience the electric field in the depletion region, which sweeps them across that region to the p side.

Similarly, some of the minority thermally generated electrons in the p type material diffuse to the edge of depletion region & get swept by electric field in the depletion region across the junction to the 'n' side.

These 2 component :-

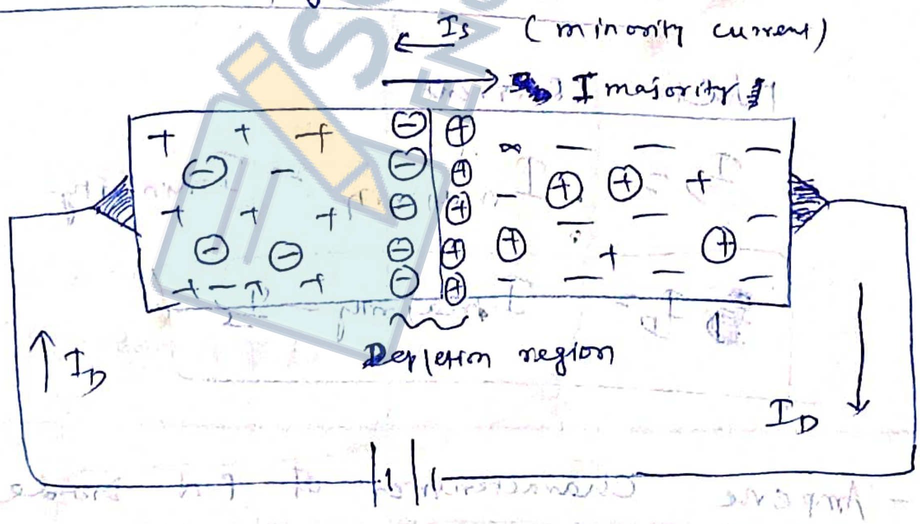
electron moved by drift from p to n

& hole " " " n to p

add together to form the reverse saturation current I_S.

In the reverse bias, the current due to majority carriers is absent only current due to minority carrier. Called Reverse saturation current. This current is saturated and always const. independent of forward or reverse biasing.

Forward Biasing :-



$$I_D = I_{majority} - I_S$$

When P type semiconductor is connected to the +ve terminal and n type semiconductor is connected to the -ve terminal of the voltage source then it is said to be forward biased.

The +ve terminal repells the holes and -ve terminal repells the electrons. These majority carriers will neutralize some of the uncovered bound charge, causing less charge to stored in the depletion layer. Thus the depletion layer narrows and the depletion barrier voltage reduces. The reduction in barrier voltage enables more holes to cross the barrier from p material into n material and more electrons from n side to p side. Thus the current I_D increases until equilibrium is achieved.

Net current

$$I_D = I_{majority} - I_{minority}$$

$$I_D = I_{majority} - I_s$$

Volt-Ampere Characteristics of P-N Diode

The voltage V_D & current I_D of a P-N junction diode is related by the following eqn

$$I_D = I_s\left(e^{V_D/\eta V_T} - 1\right)$$

Where

V_D = Diode voltage

If diode is forward biased V_D is taken +ve if diode is reverse biased V_D is taken −ve.

I_S = Reverse saturation current.

V_T = Thermal voltage or Volt equivalent of temperature.

$= \frac{KT}{q} \simeq 26\ mV$ at Room temp.

K = Boltzman's Const = 1.38×10^{-23} J/K.

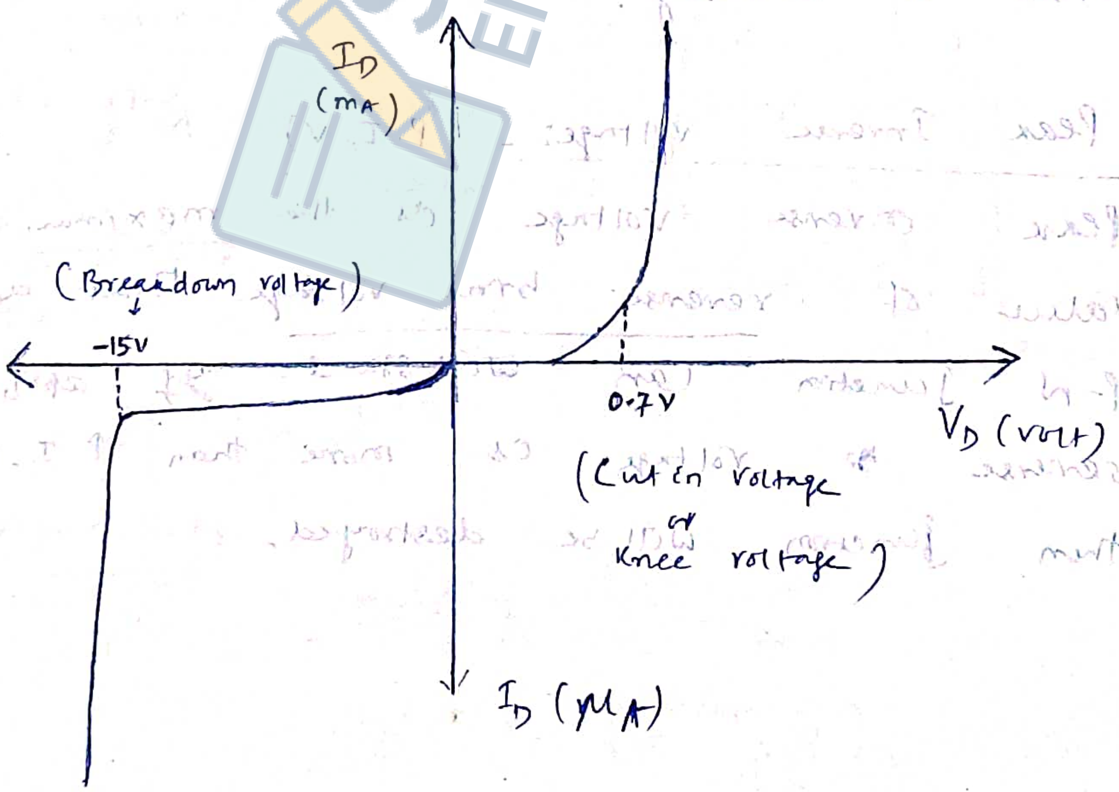
q = Charge of electron = 1.6×10^{-19} C.

T = Absolute temp

η = Recombination factor

= 1, for Ge

= 2, for Si



→ It is clear that current in semiconductor diode rises exponentially with applied forward bias.

Knee voltage or Cut in voltage

Knee voltage or Cut-in voltage is that value of forward voltage at which current through the junction starts rising sharply.
The value of knee voltage is approximately 0.3V for Ge & 0.7V for Si.

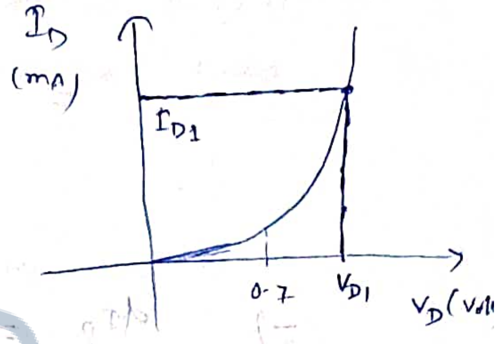
→ Current in reverse bias region is called Reverse saturation current and its magnitude is very less. But when go on increasing reverse voltage then at a particular value of reverse voltage called reverse breakdown voltage, current in diode rises sharply.

Peak Inverse voltage - (P.I.V)

Peak inverse voltage is the maximum value of reverse bias voltage that a P-N junction can withstand. If applied reverse voltage is more than P.I.V then junction will be destroyed.

Resistance Levels

1) Static or DC Resistance



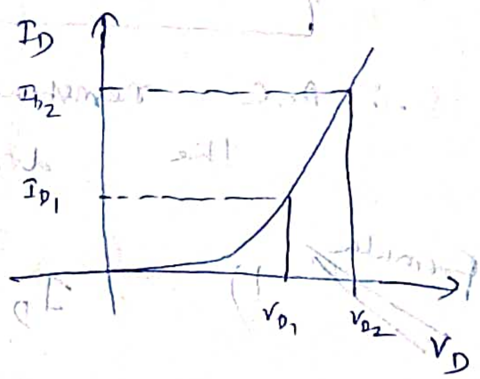
The static or DC resistance can be obtained by choosing any point on the curve and taking the ratio of the voltage & current corresponding to that point.

$$R_D = \frac{V_{D1}}{I_{D1}}$$

2) Dynamic or AC resistance:-

It is defined as the ratio of change in voltage across the diode to the change in current produced in the diode.

$$r_d = \frac{\Delta V_d}{\Delta I_d}$$



In the figure:-

$$r_d = \frac{V_{D2} - V_{D1}}{I_{D2} - I_{D1}}$$

Mathematically

~~$I_D = I_s\left(e^{V_D/\eta V_T} - 1\right)$~~

$$I_D = I_s\left(e^{V_D/\eta V_T} - 1\right)$$

$$\Rightarrow \frac{dI_D}{dV_D} = \frac{d}{dV_D} I_S\left(e^{V_D/\eta V_T} - 1\right)$$

$$= I_S\left[e^{V_D/\eta V_T} \cdot \frac{1}{\eta V_T}\right]$$

$$\Rightarrow \frac{dI_D}{dV_D} = \frac{I_S e^{V_D/\eta V_T}}{\eta V_T}$$

$$= \frac{I_D + I_S}{\eta V_T}$$

$\because I_D = I_S(e^{V_D/\eta V_T} - 1)$

$= I_S e^{V_D/\eta V_T} - I_S$

$\Rightarrow I_D + I_S = I_S . e^{V_D/\eta V_T}$

Since $I_D >> I_S$

$$\Rightarrow \frac{dI_D}{dV_D} \simeq \frac{I_D}{\eta V_T}$$

$$\Rightarrow \boxed{\frac{dV_D}{dI_D} = r_d = \frac{\eta V_T}{I_D}}$$

$\therefore$ A.C resistance varies inversely with the diode current.

Formula 1) $I_D = I_S\left(e^{V_D/\eta V_T} - 1\right)$

$I_D \simeq I_S e^{V_D/\eta V_T}$ $\because I_S$ is very small

$$\Rightarrow \frac{I_D}{I_S} = e^{V_D/\eta V_T}$$

$$\Rightarrow \boxed{I_S = I_D e^{-\frac{V_D}{\eta V_T}}}$$

Q/ A silicon diode said to be 1 mA device displays a forward voltage of 0.7 V at current of 1 mA. Evaluate the junction scaling constant I_S in the event that η is either 1 or 2.

Ans :- $I_S = I_D \, e^{-\frac{V_D}{\eta V_T}}$

$\because \eta = 1$, $V_T = 25\,mV$

for $\eta = 1$ (Ge), $I_S = 10^{-3} \times e^{-\frac{0.7}{1 \times 25 \times 10^{-3}}}$

$= 10^{-3} \times e^{-\frac{700}{25}}$

$I_S = 6.9 \times 10^{-16}\,A$

for $\eta = 2$ (Si) $\quad I_S = 10^{-3} e^{-\frac{700}{2 \times 25}}$ $\quad \eta = 2$, $V_T = 25\,mV$

$\Rightarrow I_S = 8.3 \times 10^{-10}$ Amp.

~~2/ $I_S = I_D \, e^{-\frac{V_D}{\eta V_T}}$~~

Derivation :-

$I = I_S \left(e^{V_D/\eta V_T} - 1\right)$

~~$I_1 = I_S \left(e^{V_1/\eta V_T} - 1\right)$~~

$I \simeq I_S \, e^{V_D/\eta V_T}$

Let $I_1 = I_S \, e^{V_1/\eta V_T}$

$I_2 = I_S \, e^{V_2/\eta V_T}$

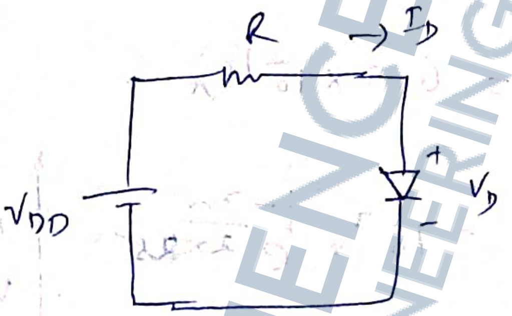
$$\frac{I_2}{I_1} = e^{\frac{V_2 - V_1}{\eta V_T}}$$

$$\Rightarrow \ln\left(\frac{I_2}{I_1}\right) = \frac{V_2 - V_1}{\eta V_T}$$

$$\Rightarrow V_2 - V_1 = \eta V_T \ln\left(\frac{I_2}{I_1}\right)$$

$$\Rightarrow V_2 - V_1 = 2.3 \eta V_T \log\left(\frac{I_2}{I_1}\right)$$

Q/ Example 3.4



Determine the current I_D and diode voltage V_D. Given $V_{DD} = 5V$, $R = 1 k\Omega$. Assume that diode has current of 1 mA at voltage of 0.7V. and the voltage drop changes by 0.1 V for every decade change in current.

Ans:
$$I_D = \frac{V_{DD} - V_D}{R} = \frac{5 - 0.7}{1 k\Omega}$$

$$I_D = 4.3 mA$$

$$V_2 - V_1 = 2.3\, \eta V_T \log\left(\frac{I_2}{I_1}\right)$$

Given, $V_2 - V_1 = 0.1$

$\frac{I_2}{I_1} = 10$ (decade change in current)

$\Rightarrow 0.1 = 2.3\, \eta V_T \log 10$

$\Rightarrow$ $0.1 = 2.3\, \eta V_T$

$\therefore V_2 - V_1 = 2.3\, \eta V_T \log\left(\frac{I_2}{I_1}\right)$

~~$\Rightarrow 0.1 = 0.1 \log ($~~

$\Rightarrow V_2 - 0.7 = (0.1) \cdot \log\left(\frac{4.3}{1}\right)$

$\Rightarrow V_2 = 0.7 + 0.0633$

$V_2 = .7633\ V$

The result of first iteration are $I_D = 4.3$ mA, $V_D = 0.763$ V.

For second iteration

$$I_D = \frac{5 - .763}{1} = 4.237 \text{ mA}$$

$$V_2 = 0.763 + 0.1 \ln\left(\frac{4.237}{4.3}\right)$$

$$= 0.762 V.$$

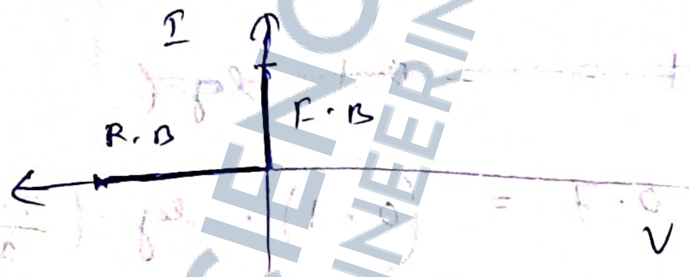
Since these values are not much

different from first iteration, no further iterations are necessary.

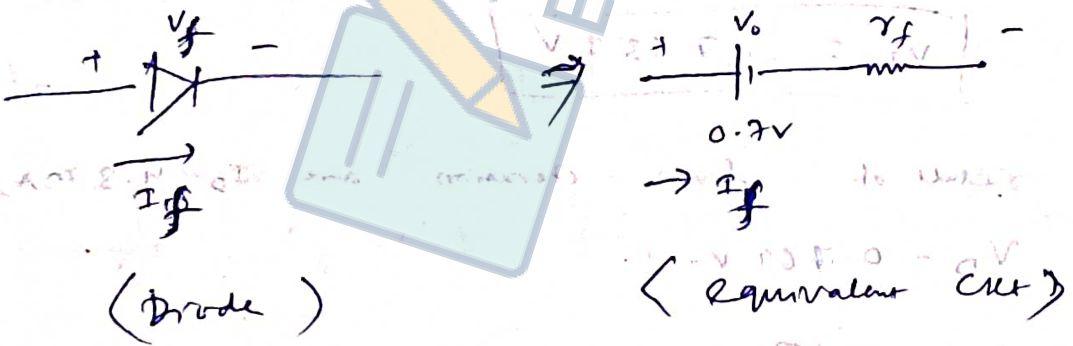
$$\therefore \boxed{I_D = 4.237\,mA, \quad V_D = 0.762\,V}$$

Ideal diode Model :- (switch)

In the application, that involves voltages much greater than the diode voltage drop (0.6 – 0.8 V), we may neglect the diode voltage drop ~~althoug~~ altogether while calculating the diode current. This result in ideal-diode model.



Diode equivalent ckt.



The diode can be considered as a voltage source with forward resistance in series,

$$\boxed{V_f = V_0 + I_f r_f}$$

Space Charge or Transition Capacitance:

Capacitance possessed at P-N Junction when P-N junction is reverse biased is called space charge or transition capacitance and is denoted by C_T.

$$C_T = \frac{\epsilon A}{d}$$

$$= \frac{\epsilon A}{W}$$

ϵ → dielectric const.

A = Area of junction

W = width of depletion layer.

In reverse bias, 'W' width of depletion layer increases. So the transition capacitance decreases.

Diffusion or Storage Capacitance

Capacitance possessed at P-N junction when P-N junction is forward biased is called diffusion or storage capacitance and is denoted by C_D.

$$C_D = \frac{\epsilon A}{W}$$

In F.B, the width of depletion layer decreases, so C_D increases with increase in forward bias.

Zener diode :- ( like Z)

→ It is a reverse biased heavily doped silicon p-n junction diode.

→ 'Si' is prefered over Ge because of its high temperature and current capacity.

→ When diode breakdown occures both Zener & Avalance effect are present. although usually one or other dominates depending upon the reverse voltage.

→ At reverse voltage less than (say 6 V), Zener effect predominates where above 6V, Avalanche effect is predominant.

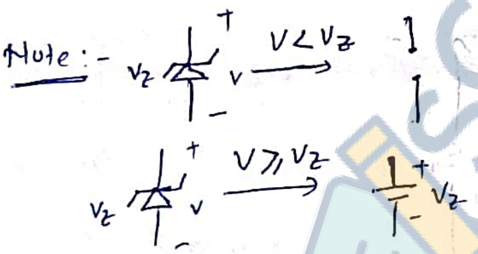
Zener breakdown	Avalanche breakdown
1) This form of breakdown occures in junction which is heavily doped.	1) This form of breakdown occures in junction which is lightly doped.
2) Due to heavy doping the depletion layer is narrow.	2) Due light doping the depletion layer is wider.
3) Due to strong electric field in the narrow region, the electric field	3) Due to high electric field, the thermally generated minority carriers collide with the semiconductor atoms in the depletion region.

is strong enough to break the covalent bond there by generating e-h pairs. Even a small increase in reverse voltage is capable producing large no. of current carriers.

4) It occurs at relatively low voltage (say -6V)

5) It is due to the direct rupture of covalent bond

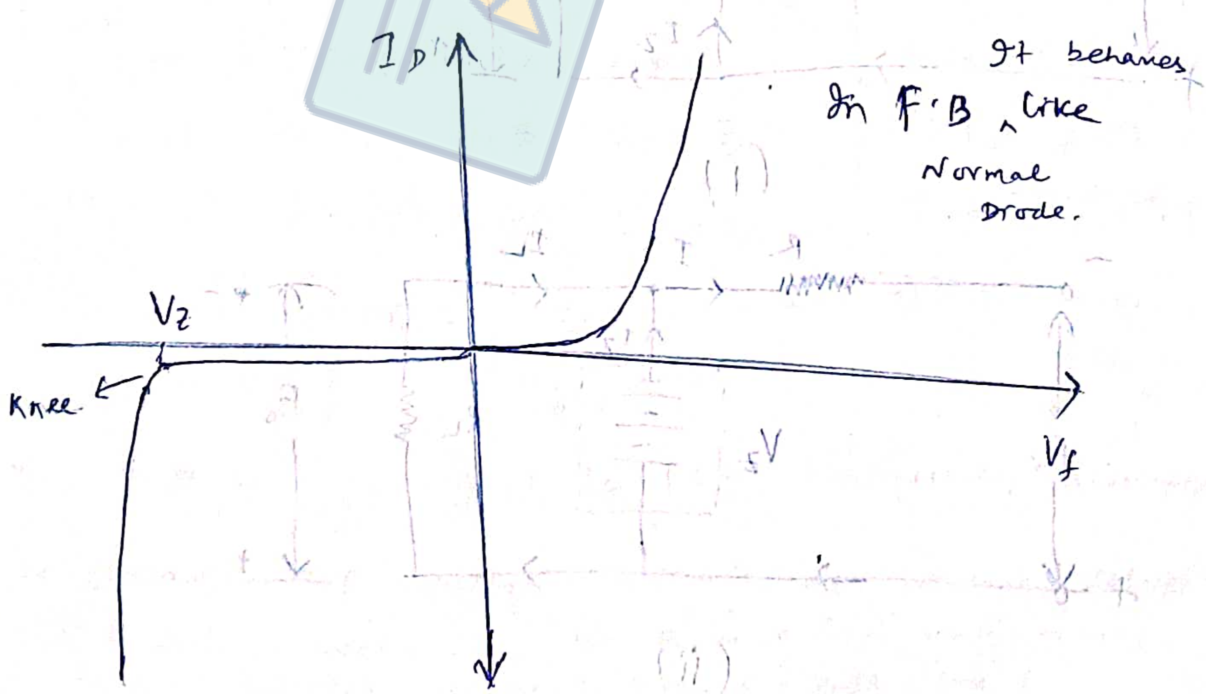
Note:-



Upon collision ~~valence~~ covalent bond breaks & e-h pair generated. The newly generated charge carriers are also accelerated by electric field resulting in more collision & hence further production of charge carriers. This leads to avalanche (flood) of charge carriers. So current rises sharply.

4) occurs at high voltage (say >6V)

5) It is due the ~~back~~ phenomenon 'impact ionization'.
(Above cummulative process of collision is called impact ionization)



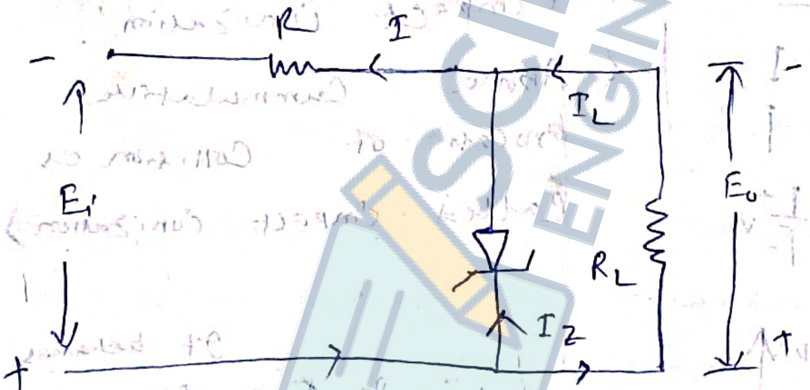
Zener diode ~~must be~~ is always 'Reverse biased' for working as a voltage regulator.

Appl^n of Zener diode

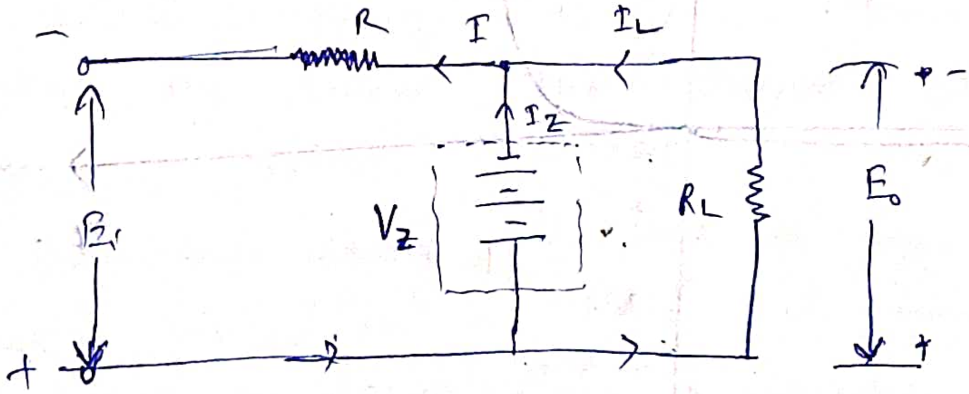
1) As a voltage regulator
2) As a peak clipper
3) For meter protection against damage from accidental application of excessive voltage.

Zener diode as voltage stabiliser:-

A Zener diode can be used as a voltage regulator to provide a constant voltage from a source whose voltage may vary over sufficient range.



(i)



(ii)

Zener diode of Zener voltage V_Z is reverse connected across the load R_L across which constant o/p is desired.

Case-I (Suppose the i/p voltage increases)

Since the Zener is in breakdown region, the Zener diode is equivalent to a battery V_Z (as shown in fig ii). It is clear that o/p voltage remains constant at V_Z. The excess voltage is dropped across the series resistance R. This will cause an increase in the value of total current I. The Zener will conduct the increase of current in I (low resistance path), while the load current remains constant. Hence the o/p voltage E_0 remains constant irrespective of change in i/p voltage E_i

Case-II (~~...~~ changed) (R_L changed)

If R_L decreased, this will cause load current to increase.

Voltage drop across R is $E_i - E_0$

Current $I = I_Z + I_L$

$$R = \frac{E_i - E_0}{\downarrow I_Z + I_L \uparrow}$$

$E_i - E_0 - IR = 0$

$\Rightarrow E_0 = E_i - IR$

$\Rightarrow E_0 = E_i - (I_L + I_Z)R$

$\Rightarrow R = \frac{E_i - E_0}{I_L + I_Z}$

The Zener current I_Z is automatically decreased to make o/p voltage remain at constant value.

($\because$ $E_i \to$ const, E_0 depend on I_L, but R is a fixed quantity, to maintain 'R', $I_L \uparrow$, $I_Z \downarrow$ to make I const, $E_0 = E_i - IR$ = const.)

LED (Light Emitting Diode)

→ LED: fabricated the PN junction using a semiconductor of type known as Direct band gap material (ex: GaAs)

Not required
* Note:- Direct bandgap / Indirect band gap

The minimal energy state in the conduction band and the maximum energy state in the valence band are each characterized by certain K-vector in the Brillouin zone. If the K-vector are same, it is called "direct band gap". If they are different it is called "Indirect band gap".

→ It is always forward biased

In F.B PN Jn minority carriers are injected across the junction and diffuse into P & n region. The diffusing minority carriers then recombine with majority carriers. Such recombination can be made to give rise to light emission.

LED:- operate in
→ Forward voltage 2V, 5 to 10 mA current

→ Depending upon the material used, the color of light emitted differs.

GaAsP → orange/yellow.

GaP → Green.

→ Cut in voltage 1.3 V

→ wave length of the light emitted

$$\lambda = \frac{1.24}{E_g} \mu m$$

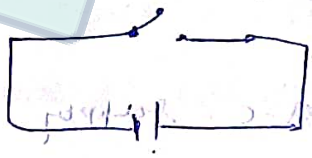
E_g = in eV (electron volt)
= Energy gap.

Diode As a switch

1) During F.B, ckt is short ckted (Closed ckt)

So switch is on.

2) During R.B, ckt is open ckted,
~~open ckt~~



So switch is off.

Rectifier

Soft/ hard copy ?

→ A rectifier converts A.C to D.C
Ex- Laptop adaptor
- Mobile charger.

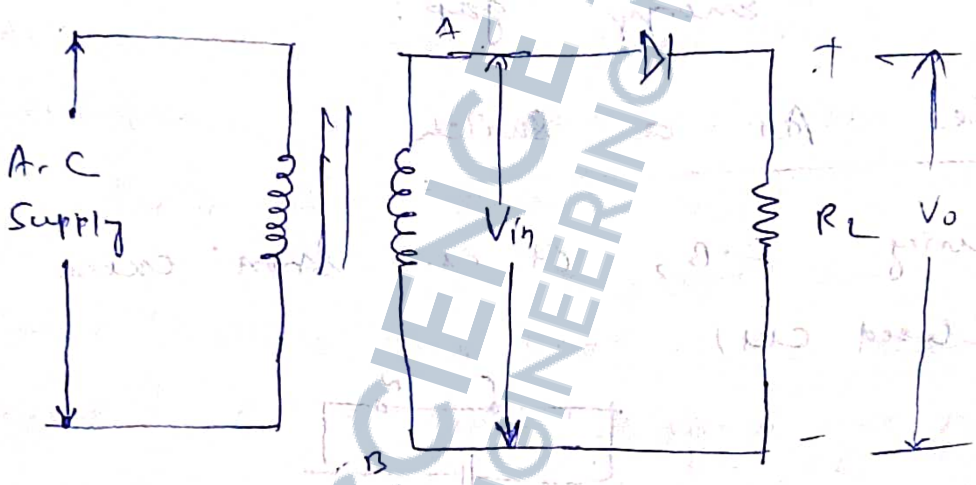
| Electronic device operate on D.C
| → Power supply in home A.C
230 V A.C → 12 V D.C (Laptop)
→ 5V (Mobile)

→ Types of rectifier

(i) Half wave rectifier

(ii) Full wave rectifier
- Center tapped rectifier
- Bridge rectifier

Halfwave Rectifier :-



→ The ckt shows, a single crystal diode acts as a halfwave rectifier.

→ The A.C supply to be rectified is applied in series with diode & load resistance R_L

→ Generally A.C supply is given through transformer.

Using transformer we have 2 advantage

1) It allows us to step up or step down the A.C voltage as situation demands

2) Secondly the transformer isolates the rectifier ckt from power line and thus

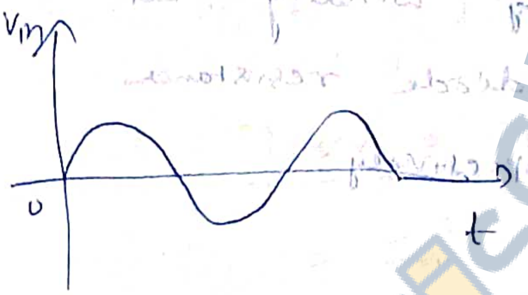
reduces the risk of electric shock.

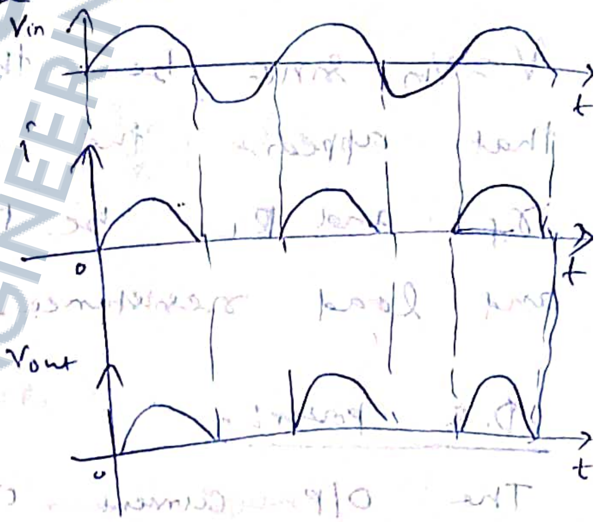
Operation :-

The A.C voltage across the secondary winding AB changes polarities after every half cycle.

→ During the +ve half cycle of input A.C voltage end 'A' becomes +ve w.r.to B. This makes diode forward biased and hence it conducts current.

→ During the -ve half cycle end A is -ve w.r.to B, under this condition the diode is reverse biased and it conducts no current.





→ Therefore, current flows through the diode during +ve half cycle i/p A-C voltage only, and blocked during -ve half cycle.

→ The d.c o/p obtained across RL.

(Pulsating d.c)

Disadvantage :-

1) The pulsating current in the load contains alternating component whose basic frequency equal to supply freq. So elaborate filtering is required.

2) A.C supply delivers power only half the time. Therefore o/p is low. So efficiency is low.

Efficiency of Half-wave Rectifier

The ratio of d.c power o/p to the applied a.c power is known as rectifier efficiency.

Rectifier efficiency, $\eta = \frac{\text{d.c power o/p}}{\text{I/P A.C power}}$

Consider a half wave rectifier, Let $V = V_m \sin\theta$ be the alternating voltage that appears the secondary winding. Let r_f and R_L be the diode resistance and load resistance respectively.

D.C power:-

The o/p current is pulsating direct current. Therefore, in order to find d.c power, average current has to be find out.

$$I_{av} = I_{dc} = \frac{1}{2\pi}\int_0^{\pi} i\, d\theta$$

$$= \frac{1}{2\pi}\int_0^{\pi} \frac{V_m \sin\theta}{r_f + R_L}\, d\theta$$

$$= \frac{1}{2\pi}\,\frac{V_m}{r_f + R_L}\int_0^{\pi} \sin\theta\, d\theta$$

$$\Rightarrow I_{dc} = \frac{1}{2\pi} \cdot I_m \cdot \int_0^{\pi} \sin\theta \, d\theta \qquad \therefore I_m = \frac{V_m}{r_f + R_L}$$

$$= \frac{I_m}{2\pi} \left(-\cos\theta\right)\Big]_0^{\pi}$$

$$= \frac{I_m}{2\pi} \cdot \left[-\left(\cos\pi - \cos 0\right)\right]$$

$$= \frac{I_m}{2\pi} \cdot \left[-\left(-1 - 1\right)\right]$$

$$= \frac{I_m}{2\pi} \times 2$$

$$I_{dc} = \frac{2 I_m}{2\pi}$$

$$\boxed{I_{dc} = \frac{I_m}{\pi}}$$

D.C power $= I_{dc}^2 R_L = \left(\frac{I_m}{\pi}\right)^2 \cdot R_L$.

A.C power o/p

$$P_{AC} = I_{rms}^2 (r_f + R_L)$$

To find I_{rms} (root mean square)

$$I_{rms} = \sqrt{\frac{1}{2\pi} \int_0^{\pi} i_L^2 \, d(\omega t)}$$

$$= \sqrt{\frac{1}{2\pi} \int_0^{\pi} I_m^2 \sin^2\omega t \, d(\omega t)}$$

$$= \sqrt{\frac{1}{2\pi} \times I_m^2 \int_0^{\pi} \left(\frac{1 - \cos 2\omega t}{2}\right) d(\omega t)}$$

$$\Rightarrow I_{rms} = \sqrt{\frac{I_m^2}{4\pi}\left(\omega t - \frac{\sin 2\omega t}{2}\right)_0^{\pi}} \quad \Big|\ \omega t = \theta$$

$$= \sqrt{\frac{I_m^2}{4\pi}\left[\ \right]}$$

$$\Rightarrow I_{rms} = \sqrt{\frac{I_m^2}{4\pi} \int_0^{\pi} \left(1 - \cos 2\theta\right) d\theta} \quad \Big|\ \text{Let } \omega t = \theta$$

$$= \sqrt{\frac{I_m^2}{4\pi}\left(\theta - \frac{\sin 2\theta}{2}\right)_0^{\pi}}$$

$$= \sqrt{\frac{I_m^2}{4\pi}\left[(\pi - 0) - (0 - 0)\right]}$$

$$= \sqrt{\frac{I_m^2}{4\pi} \times \pi}$$

$$\boxed{I_{rms} = \frac{I_m}{2}}$$

$$P_{ac} = I_{rms}^2 \left(r_f + R_L\right)$$

$$P_{ac} = \frac{I_m^2}{4}\left(r_f + R_L\right)$$

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{\frac{I_m^2}{\pi^2} \cdot R_L}{\frac{I_m^2}{4}\left(r_f + R_L\right)}$$

$$\Rightarrow \eta = \frac{I_m^2}{\pi^2} \times \frac{4}{I_m^2} \left(\frac{R_L}{R_L}\right) \quad \because r_f << R_L$$

$$= \frac{4}{\pi^2}$$

$$= .406$$

$$\Rightarrow \boxed{\eta = 40.6\%}$$

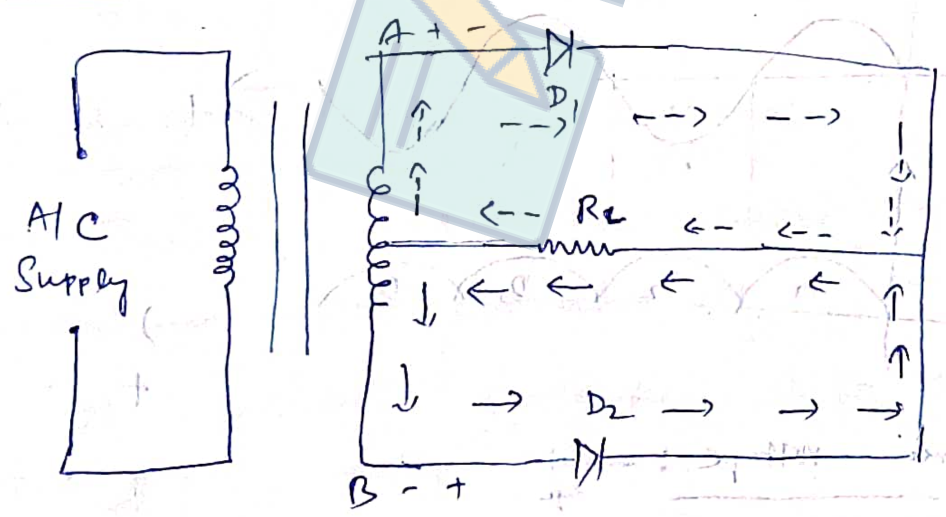
Full wave Rectifier:-

In full wave rectification, current flows through the load in the same direction for both half cycles of i/p a.c voltage.

2 types

1) Center-tap full wave Rectifier
2) Bridge rectifier

Center-tap full wave Rectifier:-



→ The ckt employs 2 diodes D_1 & D_2.

→ A center tapped secondary winding AB is used with 2 diodes connected so that each uses one half cycle of input a.c voltage.

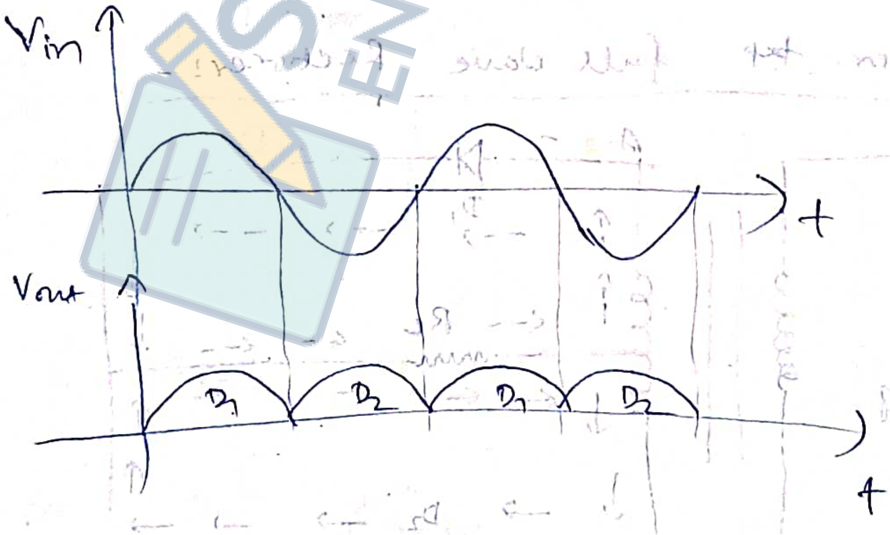
Operation :-

→ During +ve half-cycle, the point A is +ve & B is -ve, so diode D_1 conducts and D_2 is reverse biased.

→ Current flows through R_L and upper half cycle of secondary winding.

→ During -ve half cycle, the point A is -ve & point B is +ve, D_2 is forward biased, D_1 is reverse biased. The conventional current flows through D_2, R_L & low half winding.

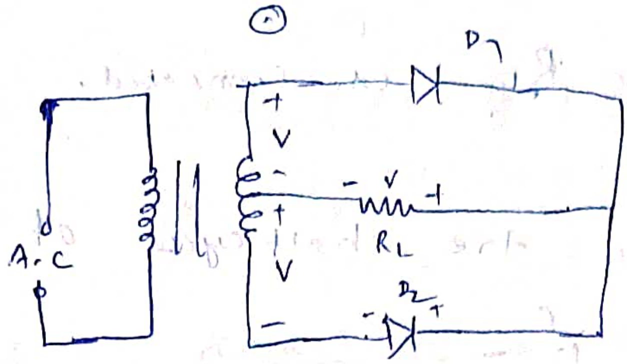
→ Current in the load R_L is same direction for both the half cycle of A.C I/P voltage.



Peak Inverse voltage :- (41) Page

As resistance of of F.B diode is small, the whole voltage V_m appears across R_L.

At one instance, D_1 conducting



D_2 is not conducting, whole secondary voltage appear across D_2. Then, voltage across R_L and voltage due to low half of secondary both appear across Diode.

i.e $V_m + V_m = 2V_m$

$\therefore$ Peak Inverse voltage $= 2V_m$.

So the diode used in this ckt should have high peak inverse voltage.

Disadvantages:-

1) In this method, It is difficult to locate the center tap on the secondary winding.
2) The diode used must have peak inverse voltage. (costly)

Full-wave Bridge rectifier:-

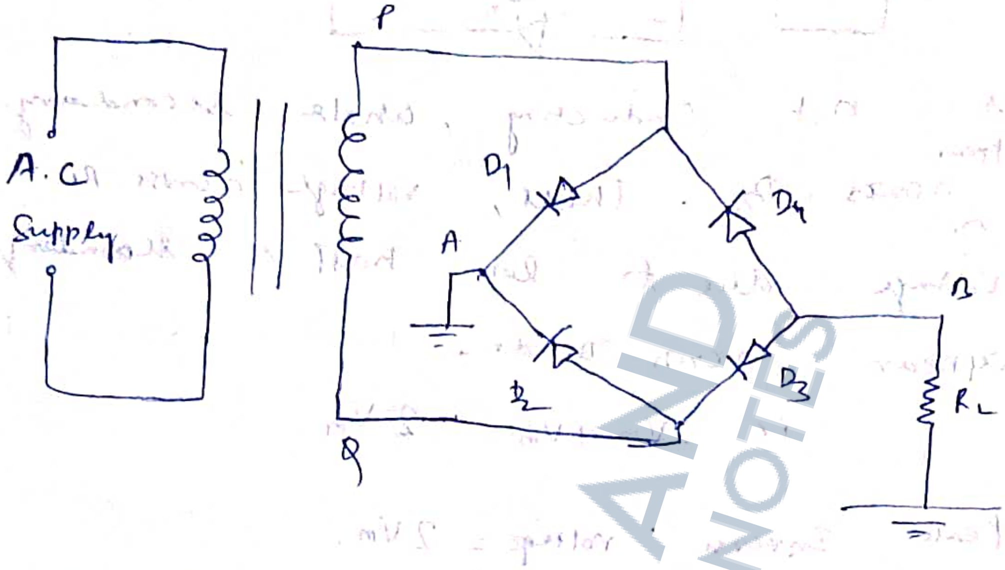
→ The need for center tapped power transformer is eliminated in the bridge rectifier.

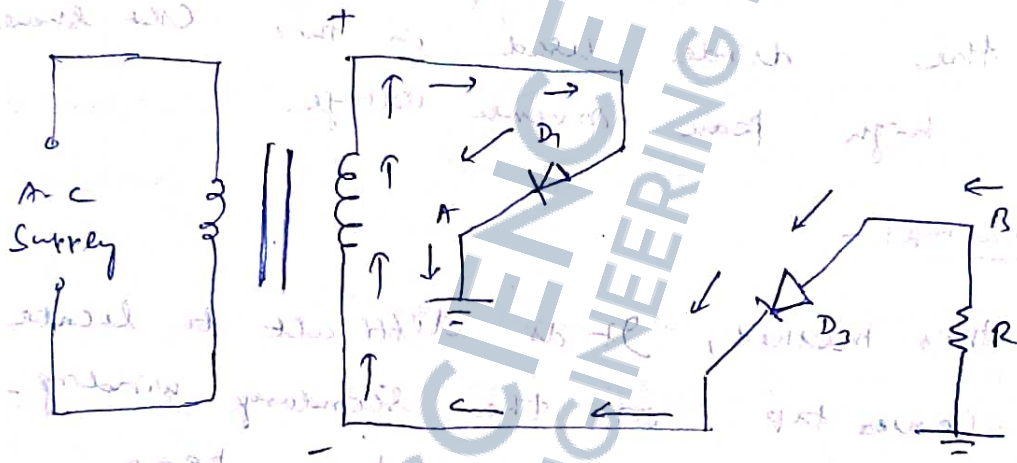
→ It contains 4 diodes D_1, D_2, D_3, D_4 connected to form bridge.

→ The A.C supply to be rectified is applied to the diagonally opposite ends of the bridge through the transformer. Between the other 2 ends of the bridge load resistance R_L is connected.

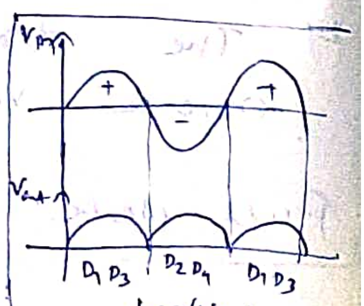
Operation :-

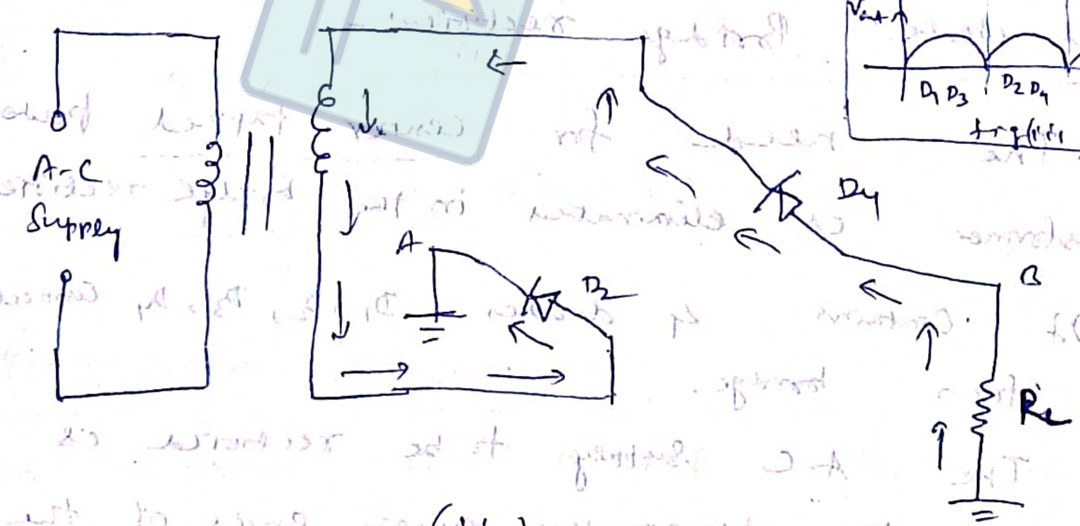
During the +ve half cycle of secondary





(i)





(ii)

voltage, the end P of the secondary winding becomes +ve and Q is -ve.

→ This makes diode D_1 & D_3 forward biased while diode D_2 & D_4 are reverse biased. Therefore only diode D_1 & D_3 conduct & these 2 diodes will be in series through load R_L as shown in fig (i). The conventional current flows from B to A through load R_L.

→ During -ve half cycle of secondary voltage, end P becomes -ve and Q is +ve. This makes only diode D_2 & D_4 forward biased where as D_1 & D_3 are reverse biased.

→ Therefore only diodes D_2 & D_4 conduct. These 2 diodes will be in series with load resistance R_L as shown in fig (ii). The conventional current flows from B to A through load R_L. i.e same direction as for +ve half cycle. Therefore, D.C o/p is obtained across load R_L.

→ Peak Inverse voltage is V_m

Advantage :-

1) The need for center-tapped transformer is eliminated.
2) The o/p is twice that of center tapp ckt for same secondary voltage.

3) The PIV (Peak Inverse Voltage) is $\frac{1}{2}$ of that center tapp ckt.

Disadvantage: -

1) → It requires 4 diodes.

2) → During each half cycle of a.c i/p 2 diodes that conduct are in series. Therefore, voltage drop in the internal resistance of rectifying unit will be twice as great as in center tap ckt. This is objectionable when secondary voltage is too small.

Efficiency of Full wave rectifier: -

Let $V = V_m \sin\theta$ be the A.C voltage to be rectified.

Let r_f & R_L be the diode resistance and load resistance respectively. The instantaneous current i is given by

$$i = \frac{V}{r_f + R_L} = \frac{V_m \sin\theta}{r_f + R_L}$$

D.C O/P Power: -

$$I_{dc} = 2 \times \frac{1}{2\pi} \int_0^{\pi} i \, d\theta$$

$$= \frac{1}{\pi} \int_0^{\pi} \frac{V_m \sin\theta}{r_f + R_L} d\theta$$

$$I_{dc} = \frac{1}{\pi} \times \left(\frac{V_m}{r_f + R_L}\right) \int_0^{\pi} \sin\theta \, d\theta$$

$$= \frac{1}{\pi} \cdot (I_m) \cdot -\cos\theta \Big]_0^{\pi}$$

$$= \frac{I_m}{\pi} \times \cos\theta \Big]_{\pi}^{0}$$

$$= \frac{I_m}{\pi} \times [1 - (-1)]$$

$$I_{dc} = \frac{2 I_m}{\pi}$$

D.C o/p power = $\left(\frac{2 I_m}{\pi}\right)^2 \cdot R_L$

A.C o/p power :-

$$P_{ac} = I_{rms}^2 (r_f + R_L)$$

$$I_{rms} = \sqrt{\frac{1}{2\pi} \times \int_0^{2\pi} i^2 \, d\theta}$$

$$= \sqrt{\frac{1}{2\pi} \times \int_0^{2\pi} I_m^2 \sin^2\theta \, d\theta}$$

$$= \sqrt{\frac{I_m^2}{2\pi} \times \int_0^{2\pi} \left[\frac{1 - \cos 2\theta}{2}\right] d\theta}$$

$$= \sqrt{\frac{I_m^2}{4\pi} \times \left(\theta - \frac{\sin 2\theta}{2}\right)\Big]_0^{2\pi}}$$

$$= \sqrt{\frac{I_m^2}{4\pi} \times [\theta]_0^{2\pi} - 0}$$

$$= \sqrt{\frac{I_m^2}{4\pi} \times 2\pi} = \sqrt{\frac{I_m^2}{2}}$$

$$\Rightarrow \boxed{I_{rms} = \frac{I_m}{\sqrt{2}}}$$

Efficiency $(\eta) = \dfrac{\text{d.c power o/p}}{\text{A.C power i/p}}$

$$= \frac{I_{rms}^2 \times R_L}{I_d}$$

$$= \frac{I_{dc}^2 \times R_L}{I_{rms}^2 (r_f + R_L)}$$

$$= \frac{I_{dc}^2 \times R_L}{I_{rms}^2 (r_f + R_L)}$$

$\because r_f << R_L$ we can neglect r_f as compared to R_L.

$$= \frac{I_{dc}^2 \times R_L}{I_{rms}^2 \times R_L}$$

$$= \frac{\left(\frac{2 I_m}{\pi}\right)^2}{\left(\frac{I_m}{\sqrt{2}}\right)^2}$$

$$= \frac{4 I_m^2}{\pi^2} \times \frac{2}{I_m^2}$$

$$= \frac{8}{\pi^2} = 0.812$$

$$\eta = 81.2\%$$

This is double that of half wave rectifier.

Ripple Factor :-

The o/p of rectifier consist of d.c component & a.c component (known as ripple). These a.c components are undesirable. The effectiveness of a rectifier depends upon the magnitude of a.c component in the o/p. Smaller this component, the more effective is the rectifier.

$$\text{Ripple factor} = \frac{\text{r.m.s value of a.c component}}{\text{value of d.c component}}$$

$$= \frac{I_{ac}}{I_{dc}}$$

$$= \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

For half wave

$$\text{Ripple factor } (\gamma) = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{I_m/2}{I_m/\pi}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{I_m}{2} \times \frac{\pi}{I_m}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{\pi}{2}\right)^2 - 1}$$

$$\boxed{\gamma = 1.21}$$

For Full wave Rectifier :-

$$\text{Ripple factor } (\gamma) = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{I_m/\sqrt{2}}{\frac{2I_m}{\pi}}\right)^2 - 1}$$

$$= \sqrt{\frac{I_m^2}{2} \times \frac{\pi^2}{4 I_m^2} - 1}$$

$$= \sqrt{\frac{\pi^2}{8} - 1}$$

$$\boxed{\gamma = 0.483}$$

Comparison :-

SL No.	Particular	Half wave	Center tap	Bridge
1.	No. of diodes	1	2	4
2.	Transformer necessary	No	Yes	No
3.	max^n efficiency	40.6 %	81.2 %	81.2 ~~40.6~~ %
4.	Ripple factor	1.21	0.48	0.48
5.	o/p freq	fin	2 fin	2 fin
6.	PIV	Vm	2 Vm	Vm

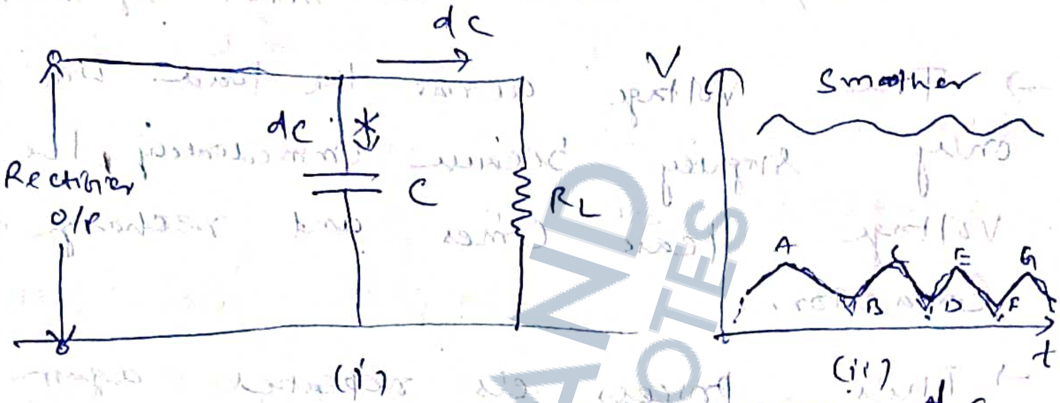
Peak Rectifier :- (Rectifier with Capacitive filter)

The impedance offered by capacitor is given by $X_C = \frac{1}{2\pi f C}$.

For dc, frequency $(f) = 0$

$\therefore X_C = \infty$.

$\therefore$ The capacitor offers infinite resistance to the d.c component and allows A-C component.



Since the rectifier o/p contains d.c as well as a.c components. The capacitor blocks d.c & bypasses A-C. So all the d.c component flows through load RL. So the d.c component is filtered out.

If (Long) question :- Fig (i) show a typical capacitor filter ckt.

→ It consists of a capacitor C placed across the rectifier o/p parallel to load RL.

→ The pulsating direct voltage of the rectifier is applied across the capacitor. As the rectifier voltage increases, it charges the capacitor & also supplies current to the load.

→ At the end of a quarter cycle (point A). The capacitor is charged to a peak value Vm of the rectifier voltage.

→ Now the rectifier voltage starts to decrease. As this occures, the Capacitor discharge through the load and the voltage across (i.e across parallel Combination of RC) decreases as shown by the line AB.

→ The voltage across the load will decrease only slightly because immediately the next voltage peak comes and recharge the Capacitor.

→ This process is repeated again & again, and the o/p voltage form becomes ABCDEFG. It is such that very little ripple is left in the o/p.

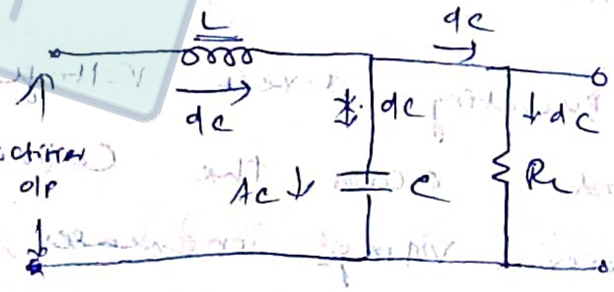
• Other filters :-

Inductor offers impedance $X_L = 2\pi f L$

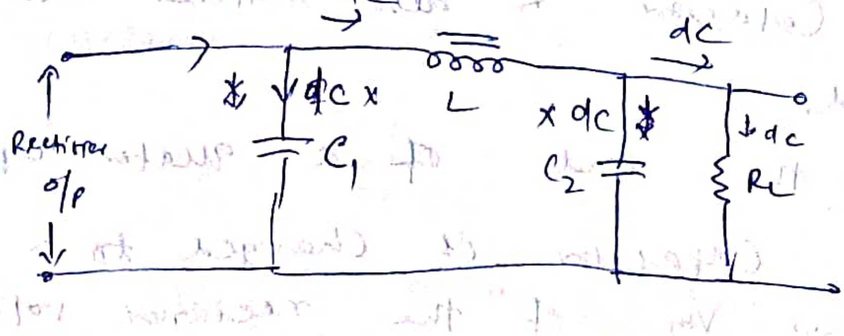
for D.C, $f = 0$, $X_L = 0$.

It passes D.C but blocks A.C.

LC filter



π filter :-



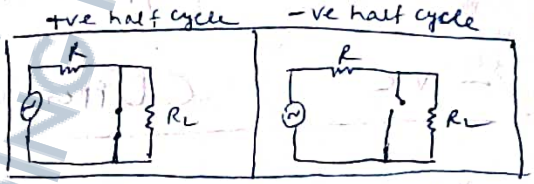
Clipper:-

→ A clipper (or limiter) is used to clip off or remove a portion of a.c signal. The halfwave rectifier is basically a clipper that eliminates one of the alternations of a.c signal.

A Clamper (or dc restorer) is used to restore or change the dc reference of an a.c signal.

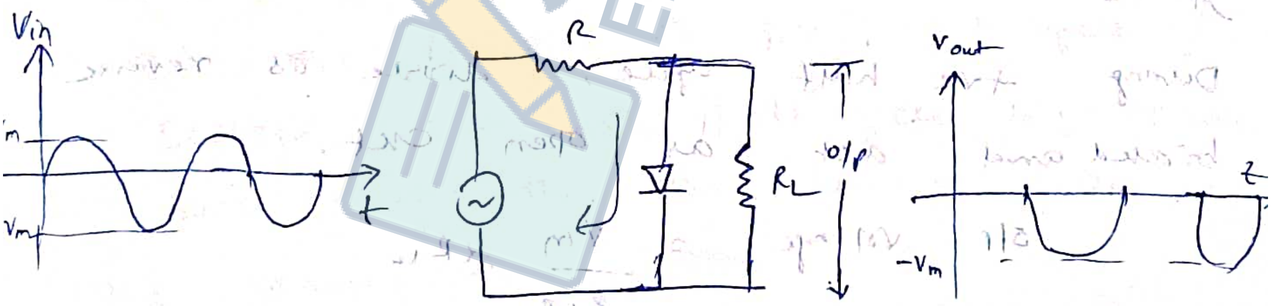
Appl'n of Clipper:- In RADAR, Digital & other electronic ckt.

+ve Clipper:-



→ A +ve clipper is that which removes the +ve half cycle of the i/p voltage.

→ As shown in fig, the o/p voltage has all the +ve half cycle removed or clipped off.



→ During the +ve half cycle of the i/p voltage, the diode is forward biased and conducts heavily. Therefore, voltage across diode (which behave as short) & hence across R_L is zero.

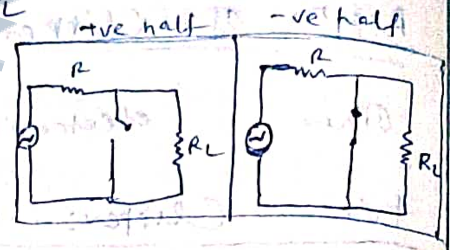
During -ve half cycle, diode is reverse biased & behave as open, In this cond", the ckt behave as voltage divider with o/p of,

$$\text{o/p voltage} = \frac{V_m}{R+R_L} \times R_L$$

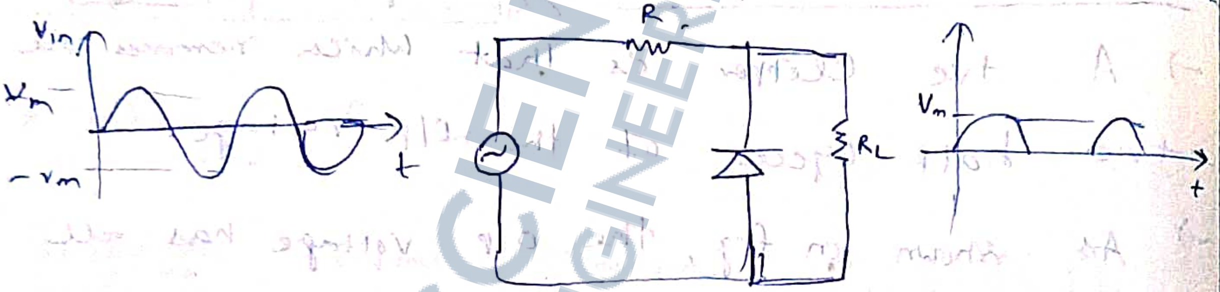
$R_L >> R$

$$\therefore \text{o/p voltage} \simeq \frac{V_m}{R_L} \times R_L$$

$$\therefore \text{o/p voltage} \simeq V_m$$



-ve Clipper :-



It is similar to that of +ve clipper

During +ve half cycle, diode is reverse biased and act as open ckt.

$$\text{o/p voltage} = \frac{V_m}{R+R_L} \times R_L$$

Since $R_L >> R$

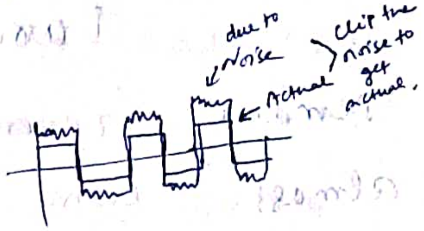
$$\text{o/p voltage} \simeq \frac{V_m}{R_L} \times R_L$$

$$\text{o/p voltage} \simeq V_m$$

During -ve half cycle

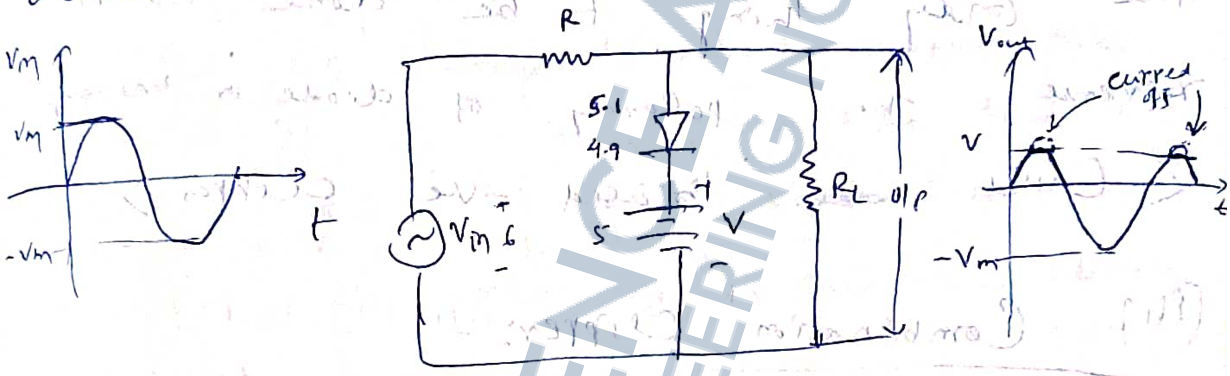
Diode is forward biased and act as short

-ucted. So the voltage across the diode i.e voltage across the load is zero. So the -ve half cycle is clipped off from the i/p.



Biased Clipper:-

Sometimes it is desired to remove a small portion of +ve or -ve half cycle of the signal, for this biased clipper is used.



The fig shows a biased clipper using a diode with battery of 'V' volts.

→ With the polarities of battery shown, a portion of +ve half cycle will be clipped, but -ve half cycle will appear as such across the load. Such a clipper is called biased +ve clipper.

→ The diode conducts heavily so long as the i/p voltage is greater than +V. When i/p voltage greater than +V, the diode behave as a short and o/p equals to +V.

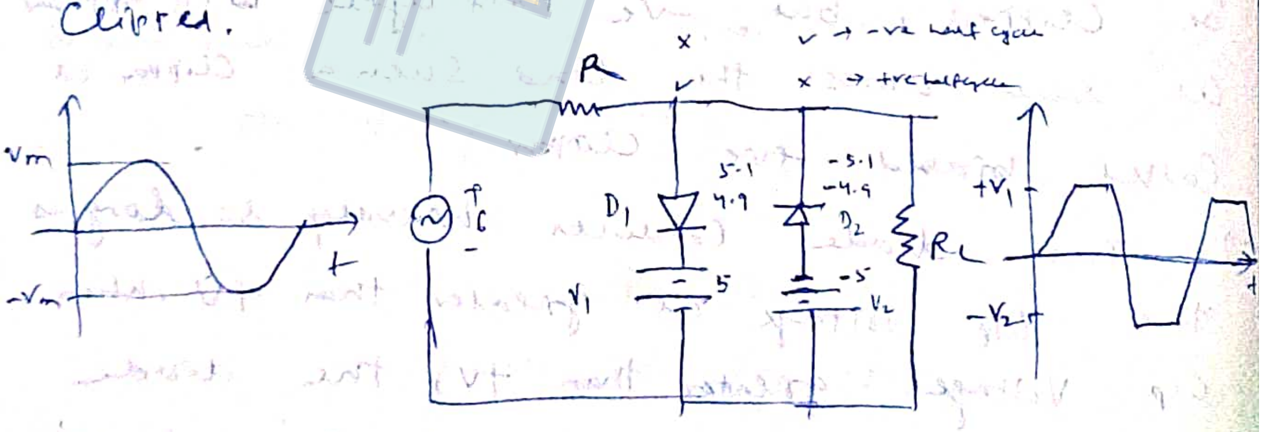
When the i/p voltage less than +V, diode is reverse biased and behave as an open. Therefore, most of i/p voltage appears across the o/p. In this way, the biased +ve clipper removes the i/p voltage above +V.

During -ve half cycle, the diode remains reverse biased, (open ckt). Therefore, almost entire -ve half cycle appears across the load.

If it is desired to clip a portion of -ve half cycle of i/p voltage, the only thing to be done is to reverse the polarity of diode or battery. < Called ~~+ve~~ biased -ve clipper >

(iii) Combination Clipper:-

It is combination of biased +ve and -ve clippers. With a combination clipper, a portion of both +ve & -ve half cycle of i/p voltage can be removed or clipped.



→ During +ve half cycle, when i/p voltage > V_1 diode D_1 conducts heavily while D_2 remain reverse biased.

Therefore, a voltage V_1 appears across the load. This o/p voltage stays at V_1 so long as i/p voltage exceeds V_1.

On other hand, during -ve half cycle, diode D_2 will conduct heavily & o/p stays at $-V_2$ as long as i/p voltage greater than $-V_2$.

Between $+V_1$ and $-V_2$ neither diode is on. Therefore in this condition, most of the i/p voltage appears across the load. It is interesting to note that this clipping ckt can give square wave o/p if V_m is much greater than the clipping levels.

Appln of Clipper:-

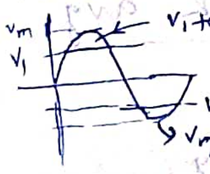
1) Changing the shape of waveform

2) Ckt transient protection.

3) Noise clipper, Noise canceller

Note !- During +ve halfcycle, D_2 is reverse biased.

For D_1, upto the i/p voltage $< V_1$, D_1 is reverse biased. The current will flow through R_L. O/p appears as V_1. When i/p voltage $> V_1$, D_1 is forward biased. O/p will be zero for V_1 to V_m.

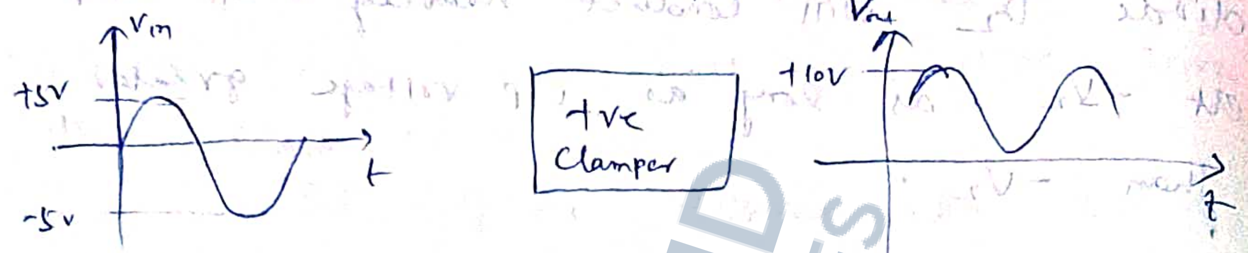


During -ve ½ cycle D_1 is reverse biased.

For D_2, up to $-V_2$, D_2 is reverse biased because P end is more -ve. So o/p will appear as it is as i/p, for V_2 to V_m N end is more -ve, so D_2 is forward biased. O/p voltage is zero for V_2 to V_m.

Clamping Ckts

✓ A ckt that places either the +ve or -ve peak of a signal at a desired d.c level is known as a clamping ckt.



→ A clamping ckt essentially adds d.c component to the signal.

→ The i/p signal is a sine wave having peak to peak value 10V. The clamper adds the d.c component and pushes the signal upwards so that -ve peak falls on the zero level.

→ Shape of original signal has not changed. Only there is a vertical shift in the signal. Such a clamper is called +ve clamper.

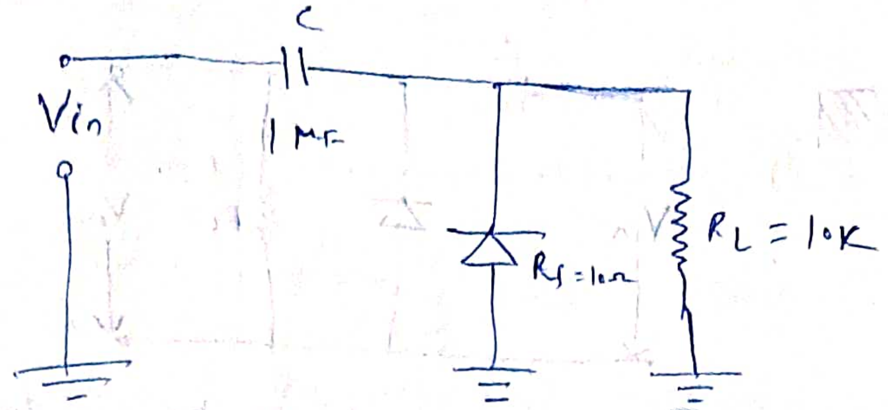
→ The -ve clamper does the reverse i.e. pushes the signal downwards so that +ve peak falls on the zero level.

(i) The clamping ckt does not change the peak to peak or rms value of the waveform.

(ii) A clamping ckt changes the peak & avg. value of the waveform.

before clamping	After clamping
Peak value = +5 V	Peak value = +10V
$Avg = \frac{+5-5}{2} = 0$	$Avg = \frac{10+0}{2} = 5V$

Basic idea of a Clamper:-



→ Clamping ckt should not change peak to peak value of the signal; it should only change the d.c level.

→ To do so, a clamping ckt uses a capacitor, together with a diode and a load resistor R_L.

→ The operation of a clamper is based on the principle that charging time of the capacitor is made very small as compared to its discharging time.

→ When diode is forward biased,

Charging time constant $\tau = R_f \cdot C = 10 \times 10^{-6}$
$= 10\ \mu s$.

Total charging time $\tau_c = 5R_fC = 5 \times 10\mu s = 50\mu s$.
(formula)

Discharging time constant $\tau = R_L \cdot C = 10 \times 10^3 \times 10^{-6}$
$= 10\ ms$

Total discharging time $= 5R_LC = 50\ ms$.

✓ It may be noted that charging time ($50\mu s$) is very small as compared to discharging time ($50\ ms$). This is the basic of clamper ckt operation.

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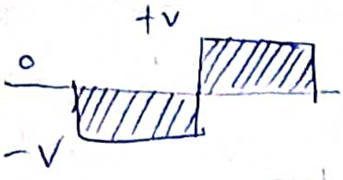
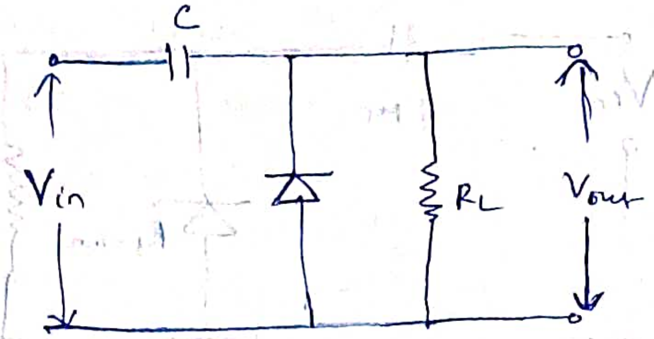
+ve Clamper :—

( point up +ve)





→ I/P signal is assumed to be a square wave with time period T.

→ The clamped output is obtained across R_L. The ckt design incorporate 2 main features

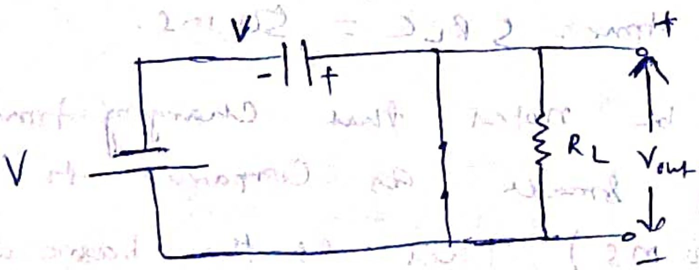
(a) The value of C & R_L are so selected that time constant $\tau = CR_L$ is very large.

This means voltage across the capacitor will not discharge significantly during the interval of diode.

(b) Secondly, $R_L C$ time const. is intentionally made much larger than time period T of the incoming signal.

Operation :- → Refer to fig (i)

(i) During -ve half cycle, of the i/p signal the diode is forward biased. The diode behaves as a short.



(i) (For -ve half cycle)

(i)

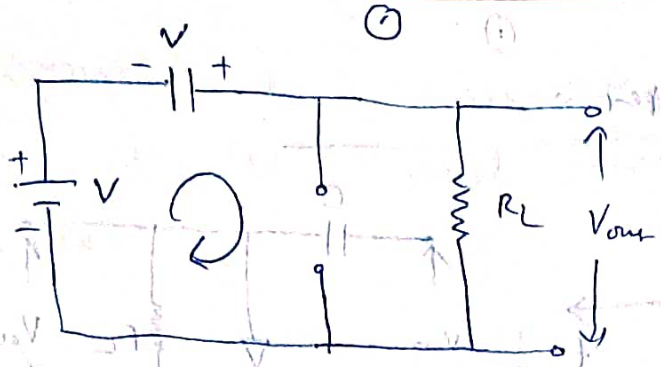


fig:- (For +ve half cycle)

→ The charging (i) time const. (= CR_f where R_f = forward resistance of the diode) is very small so that capacitor will charge to V volts quickly. It is easy to see this that during this interval, the o/p voltage will directly across the short ckt. $V_{out} = 0$.

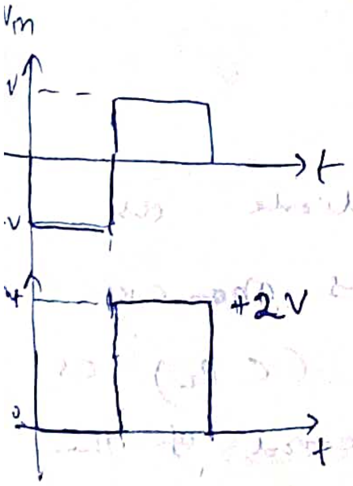
(ii) During +ve half cycle (fig ii), the diode is reverse biased and behave as an open.

Since the discharging time constant (CR_L) is much greater than the time period of the i/p signal, the capacitor remain almost full charged to 'V' volts during the off time of the diode.

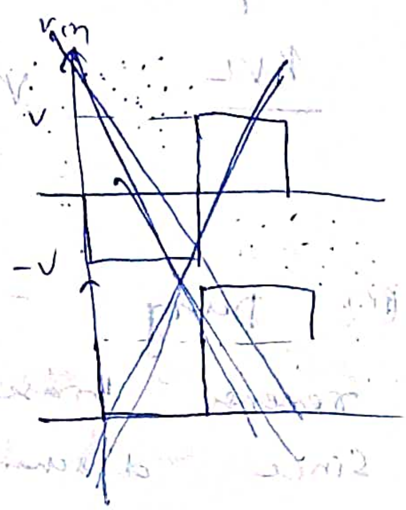
Applying Kirchhoff's voltage law.

$$V + V - V_{out} = 0$$

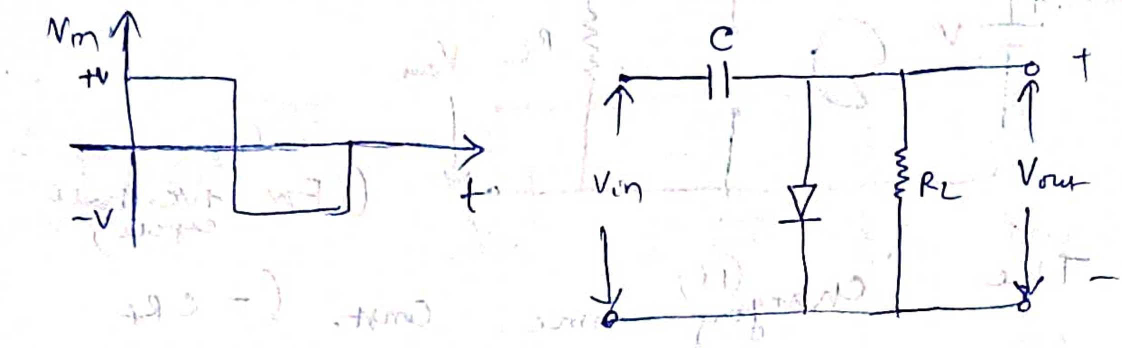
$$\Rightarrow \boxed{V_{out} = 2V}$$



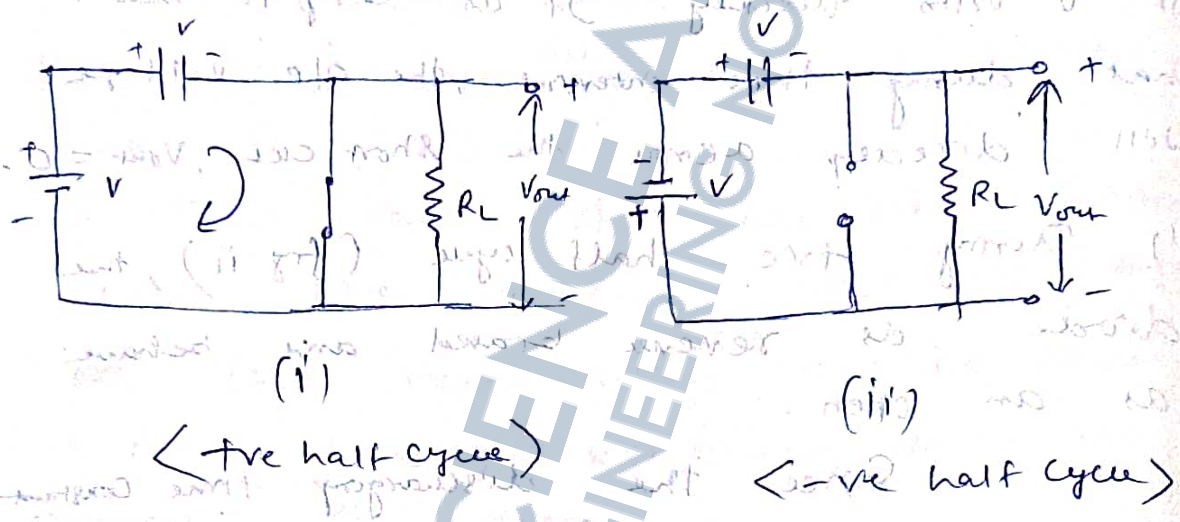
The i/p signal has been pushed upward by V volts so that −ve peak falls on the zero level.



–Ve Clamper



(i) During +ve half cycle of the i/p signal, diode is forward biased. Therefore, the diode behave as short.



The charging time constant (CRf) is small so that capacitor will charge to V volts very quickly. It is easy to see that during this interval O/P voltage is directly across the short ckt.

KVL

$$V - V - V_{out} = 0$$

$$\Rightarrow V_{out} = 0$$

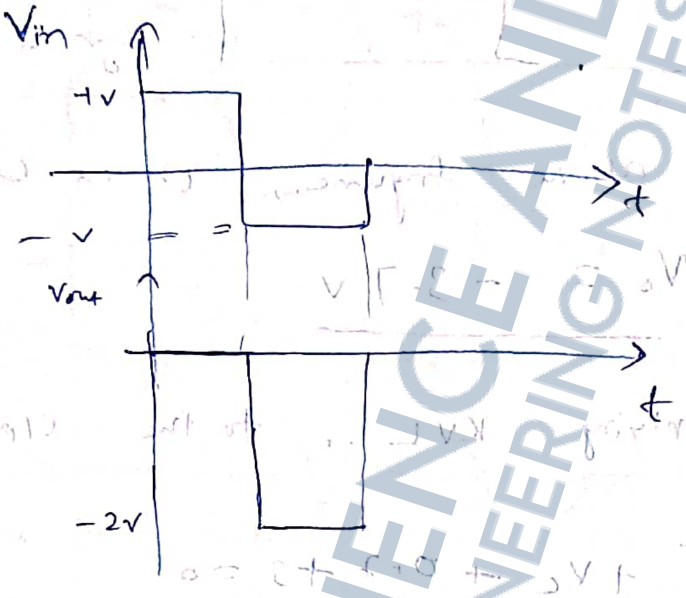
(ii) During -ve half cycle, diode is reverse biased & behave as open ckt. Since discharging time const. (C R_L) is much greater than the time period of the

I/P signal, the capacitor remains fully charged to 'V' volts during off time of the diode.

KVL

$-V - V - V_{out} = 0$

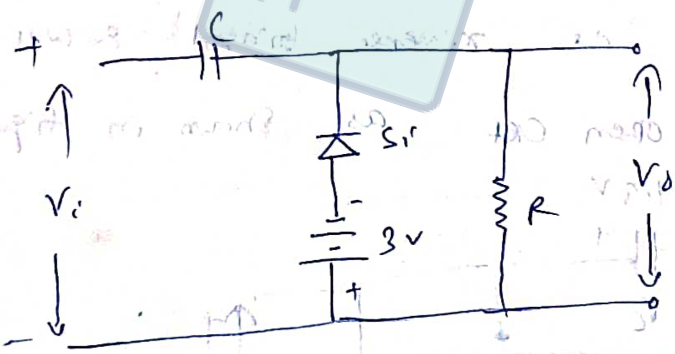
$\Rightarrow V_{out} = -2V$ volts.



Application of Clamper :-
In T.V transmitter and receiver.

BPUT 2017 Q/ Analyze & draw the o/p waveform of the following ckt when

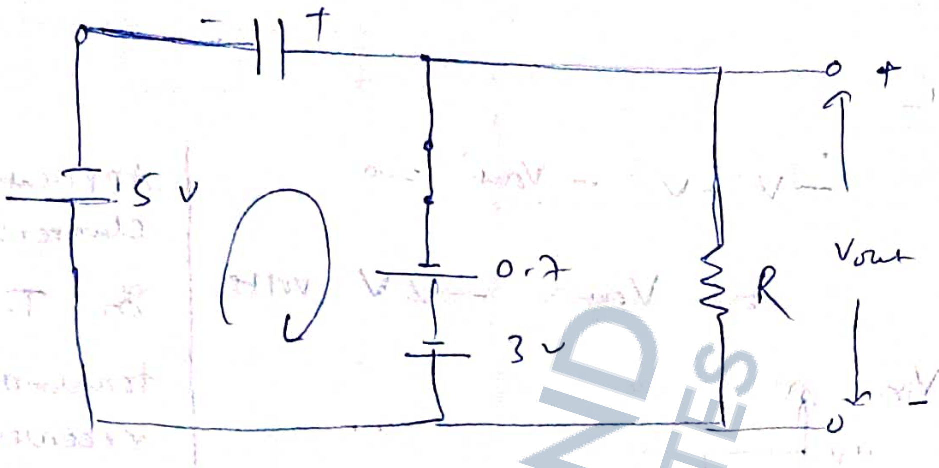
$V_i = 5 \sin(100\pi t)$.



Ans :- This is a +ve clamper ckt. The ckt can be analyzed as follows.

During the -ve half cycle of I/P signal

the diode is forward biased. The n/w (network) will appear as shown in figure



From the above figure, it is clear that

$$V_o = -3.7\ V$$

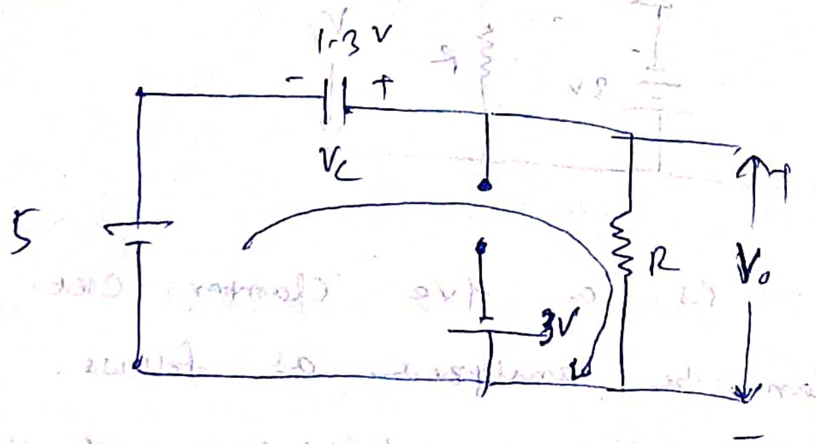
Further applying KVL, to the i/p loop,

$$-5 + V_c + 0.7 + 3 = 0$$

$$\Rightarrow V_c = 5 - 3.7 = 1.3\ V$$

∴ The capacitor will charge upto 1.3V.

During +ve half cycle of i/p signal, the diode is reverse biased & will behave as open ckt as shown in figure

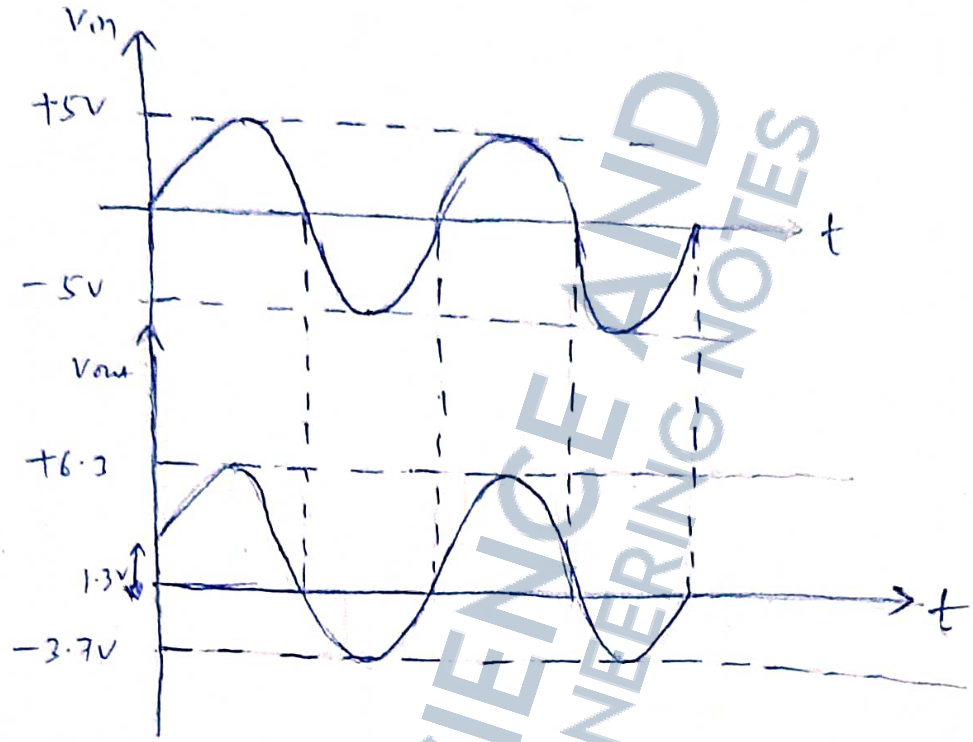


Since it is open ckt, battery has no effect.

KVL, $5 + V_C - V_{out} = 0$

$\Rightarrow 5 + 1.3 - V_{out} = 0$

$\Rightarrow V_{out} = 6.3V.$



Note:- In Vin, the peak to peak value 5+5 = 10V.

In Vout, the peak to peak value remained constant 6.3+3.7 = 10V.

— o —